Pulsewidth Modulations for the Comprehensive Capacitor Voltage Balance of $n$-Level Diode-Clamped Converters

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Abstract - In the previous literature, the introduction of the virtual space vector concept for the three-level three-leg neutral-point-clamped converter has led to the definition of pulsewidth modulation (PWM) strategies guaranteeing the dc-link capacitor voltage balance under any type of load, with the only requirement being that the addition of the three phase currents equals zero. This paper presents the definition of the virtual space vectors for the general case of an $n$-level converter, suggests guidelines for designing virtual-space-vector PWM strategies, and provides the expressions of the phase duty-ratio waveforms corresponding to this family of PWMs. Modulations defined upon these vectors enable the use of diode-clamped topologies with passive front-ends. The performance of these converters operated with the proposed PWMs is compared to the performance of alternative designs through analysis, simulation and experiments.

I. INTRODUCTION

Multilevel converters [1]–[3] have opened a door for advances in the electric-energy conversion technology. These converters present the advantages of a lower device voltage rating, a lower harmonic distortion, and higher efficiency compared to conventional two-level converters.

These converters are typically considered for high power applications, because they allow operating at higher dc-link voltage levels with the current available semiconductor technology. But they can also be interesting for medium or even low power/voltage applications, since they allow operating with lower voltage-rated devices, with potentially better performance/economical features [4], [5].

There are three basic multilevel converter topologies: diode-clamped, flying capacitor, and cascaded H-bridge with separate dc sources. Among these topologies, diode-clamped converters are especially interesting because of their simplicity: the multiple voltage levels are generated passively through a set of series-connected capacitors. (see Fig. 1). The simplest family member, the three-level converter, has been widely studied [6]–[10]. Conventional pulsewidth modulations (PWMs), based on the selection of the nearest-three space vectors (NTV), cause an unbalance of the dc-link capacitor voltages, increasing the device voltage stress and generating low-frequency output-voltage distortion [7]. In higher-level diode-clamped converters, conventional modulation solutions lead to the collapse of some capacitor voltages under a wide range of operating conditions [11], [12].

Fig. 1. Multilevel three-leg diode-clamped converters. (a) Functional diagram of an $n$-level converter. (b) Five-level converter topology.

To overcome these limitations of diode-clamped topologies, some authors propose the addition of circuitry specifically designed to guarantee the balance [13], [14]. Other authors introduce a fourth leg [15]. Finally, some authors use a back-to-back connection of multilevel converters to extend the operating range through which the balance can be guaranteed [16]–[18]. The majority of authors, though, have discarded the use of diode-clamped converters with more than three levels in favor of other topologies: flying capacitor, cascaded H-bridge with separate dc sources, and hybrid converter topologies.

The virtual-space-vector (VV) PWM presented in [10], a modulation for the three-level converter based on the definition of a set of VVs, is capable of maintaining the capacitor voltage balance for any load (linear or non-linear, balanced or unbalanced) and modulation index, provided that the addition of the output phase currents equals zero. References [19] and [20] successfully extend this concept to the four-level converter, presenting a VV PWM guaranteeing the dc-link capacitor voltage balance.

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The introduction of appropriate VVs for the three-level and four-level converter has proven beneficial, enabling the use of these converters without the need to add circuitry to maintain the balance of the dc-link capacitor voltages. This encourages exploring whether the VV concept can be extended to higher-level multilevel converters. This paper concludes that it is possible, presents the definition of such vectors for the general case of an n-level converter, and presents the phase duty-ratio expressions to easily implement the most interesting family of VV PWMs for the general n-level diode-clamped converter with two and three legs. The performance of these converters operated with the proposed PWMs is compared to the performance of these converters operated with the classical PWM algorithm computation time, dc-link capacitor voltage balance, harmonic distortion, and device switching losses. Experimental results are presented for a five-level three-leg diode-clamped converter.

II. N-LEVEL VIRTUAL SPACE VECTOR PWM

A. Virtual Space Vector Definition

In an n-level three-leg converter, \( n^3 \) switching states are available, designated as \( xyz \), where \( x, y, \) and \( z \) correspond to the dc-link points to which phases \( a, b, \) and \( c \) are connected, respectively. These switching states define \( 3^n - 3 \cdot n + 1 \) vectors in the converter space vector diagram (VDD) (see Fig. 2).

To maintain the balance of the \( n-1 \) capacitor voltages every switching cycle, we must ensure that all the average (\( V_D \)) (see Fig. 2).

The expression of these vectors in \( \alpha, \beta \) coordinates is

\[
\mathbf{V}_i = \begin{cases} \frac{2}{\sqrt{3}} & 1 \leq i \leq n-1 \\ \frac{1}{\sqrt{3}} & 1 \leq i \leq n-1 \\ \end{cases}
\]

\[
V_{ix} = \begin{cases} \frac{3+j}{\sqrt{3}} & 0 \leq i \leq n-3 \\ \frac{1}{\sqrt{3}} & 0 \leq j \leq n-3-i \\ \end{cases}
\]

\[
V_{ix} = \begin{cases} \frac{3+j}{\sqrt{3}} & 0 \leq i \leq n-4 \\ \frac{1}{\sqrt{3}} & 1 \leq j \leq n-3-i \\ \end{cases}
\]

The position of vectors \( \mathbf{V}_i \) is defined by the intersections of lines \( l_{ij} \) in \( l_{ij} \) with lines \( l_{ij} \) in \( l_{ij} \), \( \forall j, k \), where \( l_{ij} \) is the straight line joining the tip of vectors \( \mathbf{V}_i \) and \( \mathbf{V}_j \).

In terms of the switching states, virtual vector \( \mathbf{V} \) can be expressed as

\[
\mathbf{V} = \sum_{i=x}^{n} [k_i \cdot (xyz)]
\]

where \( k_i \) is the coefficient of the linear combination of switching states \( xyz \) that defines \( \mathbf{V} \). Every available switching state, except for \( 111 \) and \( nnn \), appears in at least the definition of one of these VVs. The definition of some of these vectors is

\[
V_i = \begin{cases} \frac{1}{n-2} & 222 \leq i \leq n-1 \\ \frac{1}{n-2} & 333 \leq i \leq n-1 \\ \frac{1}{n-2} & (n-1)(n-1)(n-1) \leq i \leq n-1 \\ \end{cases}
\]

\[
V_{ii} = \begin{cases} (0i1) \leq i \leq n-1 \\ (0i1) \leq i \leq n-1 \\ \end{cases}
\]

\[
V_{i(i-1)} = \begin{cases} \frac{1}{n-1} & 221 \leq i \leq n-1 \\ \frac{1}{n-1} & 322 \leq i \leq n-1 \\ \frac{1}{n-1} & (n-1)(n-1) \leq i \leq n-1 \\ \end{cases}
\]

\[
V_{i(i-2)} = \begin{cases} \frac{1}{n-2} & 221 \leq i \leq n-1 \\ \frac{1}{n-2} & 322 \leq i \leq n-1 \\ \frac{1}{n-2} & (n-1)(n-1) \leq i \leq n-1 \\ \end{cases}
\]

In general, the remaining VVs present redundancy; i.e., they can be obtained from more than one combination of switching states. The redundancy increases as the number of levels increases.

B. Virtual Space Vector Selection

The desired three-phase output voltage is represented by a reference vector (\( \mathbf{V}_{ref} = me^{\phi} \)), which is synthesized in each switching cycle by a sequence of switching states. In general, we can define a modulation strategy that maintains the balance of the capacitor voltages expressing \( \mathbf{V}_{ref} \) as a linear combination of the virtual vectors:

\[
\mathbf{V}_{ref} = d_{vz} \cdot \mathbf{V}_z + \sum_{i=1}^{n-3} d_{v_u} \cdot \mathbf{V}_{u} + \sum_{i=0}^{n-1} d_{v_{ii}} \cdot \mathbf{V}_{ii} + \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} d_{v_{ij}} \cdot \mathbf{V}_{ij}
\]

\[
0 \leq d_{i} \leq 1 \ \forall \mathbf{V}_{i}
\]

where \( d_{i} \) is the duty ratio of vector \( \mathbf{V}_{i} \). The duty ratio of switching state \( xyz \) can be then computed as

\[
d_{vz} = \sum_{i=x}^{n} k_i \cdot d_{i}
\]

where \( \mathbf{V} \) is a virtual vector defined using \( xyz \). A few simple examples of switching state duty-ratio computation are

\[
d_{332} = d_{333} = \ldots = d_{(n-1)(n-1)(n-1)} = \left[ \frac{1}{(n-2)} \right] \cdot d_{vz}
\]

\[
d_{n31} = d_{n11}
\]

\[
d_{n31} = d_{n11}
\]

A set of guidelines follow to perform the selection of VVs to approximate \( \mathbf{V}_{ref} \) in each switching cycle.

1) Select the minimum number of VVs to approximate \( \mathbf{V}_{ref} \) to reduce the number of switching transitions per switching cycle.

2) Choose VVs as close as possible to \( \mathbf{V}_{ref} \) to minimize the output voltage harmonic distortion.

3) Choose VVs whose associated switching states can be arranged to follow the sequence defined in Section II.C. This allows using pre-derived phase duty-ratio expressions in terms of the desired modulation index (\( m \)) and output line angle (\( \phi \)) similar to those presented in [10], [19], and [20] for the three- and four-level converters, and avoid performing any VVD-related computation online.

4) Choose VVs so that the final phase duty-ratio expressions are simple.
Fig. 2. First sextant of the normalized $n$-level three-leg converter VD.

Fig. 3. First sextant of the normalized $n$-level three-leg converter VVD.
C. Switching States Sequence

Finally, the sequence over time within a switching cycle of the application of the different switching states has to be decided. The chosen switching states’ order is such that each phase is connected to the dc-link points following the symmetrical sequence shown in Fig. 4. This can be achieved by simply ordering the switching-states three-digit number in descending-ascending order if appropriate VVs have been selected in the preceding Section.

Therefore, a practical implementation of a VV PWM only requires the computation of duty ratios \( d_{a_1}, d_{b_1}, d_{c_1}, d_{a_2}, d_{b_2}, d_{c_2}, \ldots, d_{a_n}, d_{b_n}, d_{c_n} \) (where \( d_p \) is the duty ratio of the phase \( x \) connection to the dc-link point \( y \)), as the addition of the appropriate switching state duty ratios calculated in Section II.B. For example, in the first sextant, to obtain \( d_{a_2} \)

\[
d_{a_2} = d_{222} + d_{221} + d_{211}.
\]

(7)

Fig. 4. Selected sequence of connection of phase \( x \) (\( a, b \) or \( c \)) to each of the dc-link points (\( 1, 2, \ldots, n \))

D. Phase-Duty-Ratio Expressions

Equation (8) presents the expressions of the phase duty-ratios corresponding to the family of VV PMWs for a three-leg diode-clamped converter.

\[
0 \leq \theta < 2\pi/3: \quad d_{a_1} = m \cdot \cos(\theta - \pi/6), \quad d_{b_1} = m \cdot \cos(\theta - \pi/2), \quad d_{c_1} = 0 \\
2\pi/3 \leq \theta < 4\pi/3: \quad d_{a_1} = 0, \quad d_{b_1} = m \cdot \cos(\theta - 5\pi/6), \quad d_{c_1} = m \cdot \cos(\theta - 7\pi/6) \\
4\pi/3 \leq \theta < 2\pi: \quad d_{a_1} = m \cdot \cos(\theta + \pi/6), \quad d_{b_1} = 0, \quad d_{c_1} = m \cdot \cos(\theta + \pi/2) \\
-\pi/3 \leq \theta < 0: \quad d_{a_1} = m \cdot \cos(\theta + 5\pi/6), \quad d_{b_1} = m \cdot \cos(\theta + 7\pi/6), \quad d_{c_1} = 0 \\
\pi/3 \leq \theta < \pi: \quad d_{a_1} = m \cdot \cos(\theta - 5\pi/6), \quad d_{b_1} = m \cdot \cos(\theta - 7\pi/6), \quad d_{c_1} = 0 \\
\pi \leq \theta < 2\pi: \quad d_{a_1} = m \cdot \cos(\theta - 5\pi/6), \quad d_{b_1} = m \cdot \cos(\theta - 7\pi/6), \quad d_{c_1} = 0 \]

(8)

\[
\sum_{i=1}^{n} d_{ai} = 1, \sum_{i=1}^{n} d_{bi} = 1, \sum_{i=1}^{n} d_{ci} = 1
\]

Actually, the average current through the inner dc-link points is zero in every switching cycle if the addition of phase currents equals zero since

\[
i_k = d_{a_1} \cdot i_a + d_{b_1} \cdot i_b + d_{c_1} \cdot i_c = d_k \cdot (i_a + i_b + i_c) = 0 \\
k = 2, 3, \ldots, n - 1
\]

(9)

An interesting particular PWM can be defined with the addition of expressions (10). Fig. 5 depicts the phase \( a \) duty-ratios for \( m = 0.75 \) and one line cycle. Phases \( b \) and \( c \) duty-ratios are the same but phase shifted \( \pm 120^\circ \), respectively. This particular PWM has two major advantages. First, since all inner dc-link point phase duty-ratios are greater than zero, we have margin in every switching cycle to regulate all capacitor dc-link voltages using the control scheme presented in [21]. Additionally, the margin to regulate is balanced since all inner dc-link point phase duty-ratios have the same value. Second, another important advantage is the simplicity of the phase duty-ratio expressions.

\[
d_{a_2} = d_{a_1} = \frac{1 - d_{a_1} - d_{c_1}}{n-2} = \frac{1 - d_{a_1} - d_{b_1}}{n-2} = \frac{1 - d_{a_1} - d_{b_1}}{n-2} \quad (i = 2, 3, \ldots, n-1)
\]

(10)

Fig. 5. Phase \( a \) duty-ratio pattern for an \( n \)-level three-leg converter.

The PWM defined by (8) and (10) corresponds to a particular VV selection. For example, Fig. 6 presents the VVD for a five-level converter. \( V_{\text{ref}} \) is approximated in every switching cycle by the three VVs defining the vertices of the triangle where it is located. The auxiliary virtual vectors \( V_A, V_B, V_C, V_D, \) and \( V_E \) are defined as a combination of certain VVs, as

\[
V_A = \frac{2}{5} V_{\text{ref}}, \quad V_B = \frac{3}{5} V_{\text{ref}}, \quad V_C = \left[ \frac{553}{442} \right] (211) - \left[ 4 \right] (53) \ 0, \ 0, \ \frac{2}{5} (53)_{x,y} \\
V_B = \frac{3}{5} V_{\text{ref}}, \quad V_C = \frac{1}{5} V_{\text{ref}}, \quad V_D = \left[ \frac{553}{442} \right] (211) - \left[ 4 \right] (53)_{x,y} \\
V_C = \frac{1}{5} V_{\text{ref}}, \quad V_D = \frac{2}{7} V_{\text{ref}}, \quad V_E = \left[ \frac{553}{442} \right] (211) - \left[ 4 \right] (53)_{x,y} \\
V_D = \frac{2}{7} V_{\text{ref}}, \quad V_E = \frac{6}{7} V_{\text{ref}}, \quad V_A = \left[ \frac{553}{442} \right] (211) - \left[ 4 \right] (53)_{x,y}
\]

(11)

The expressions in (8) and (10) allow the direct calculation of \( d_{a_1}, d_{b_1}, d_{c_1}, \ldots, d_{a_n}, d_{b_n}, \) and \( d_{c_n} \) as a function of the reference vector coordinates, without the need of identifying the triangle in which it is located and then performing calculations (4)–(7). This significantly simplifies the computations.

Fig. 6. VVD for the five-level three-leg converter.
The particular PWM defined by (8) and (10) presents 3n−5 pairs of switching transitions (one switch turns off and another turns on) per half switching cycle in all regions of the VVD. Other PWM solutions verifying (8) may present lower number of switching transitions and lower ac-side harmonic distortion (see examples in [19] for a four-level converter) but they will not be considered here for the sake of simplicity.

E. Two-Leg Converter

A similar process can be followed to derive PWM solutions that guarantee dc-Link voltage balance in a two-leg converter with \( i_2 + i_3 = 0 \) (source or load connected in between the two leg output terminals). The expressions defining the family of VV PWMs are:

\[
\begin{align*}
-2 \pi/3 \leq \theta < -\pi/3: & \quad d_{a1} = d_{a2} = 0; \\
\pi/3 \leq \theta < 2\pi/3: & \quad d_{a1} = d_{a2} = m \cdot \cos(0 + \pi/6) \\
\pi/3 < \theta < 2\pi/3: & \quad d_{a1} = d_{a2} = m \cdot \cos(0 + 7\pi/6); \\
\theta = 2\pi/3: & \quad d_{a1} = 0, \\
\text{for } i = 2, 3, \ldots, n-1
\end{align*}
\]

\[
\sum_{j=1}^{3} d_{aj} = 1; \sum_{j=1}^{3} d_{bj} = 1
\]

An interesting particular PWM is obtained with

\[
d_{a1} = d_{a2} = \frac{1 - d_{a3} - d_{a4}}{n - 2} = \frac{1 - d_{a3} - d_{a4}}{n - 2}
\]

\[
\sum_{j=2}^{n-1} d_{aj} = 1
\]

III. SIMULATION RESULTS

In this section, the performance of a three-leg diode-clamped converter connected to a single dc bus through terminals 1 and \( n \) and operated with the proposed VV PWM is analyzed through simulation in Matlab-Simulink and compared to other alternative design solutions. The dc bus can be generated, for instance, from the mains or other ac sources employing a simple diode rectifier.

Fig. 7 shows the results of the dc-link capacitor voltage balance in a five-level converter. A particular NTV PWM is used as a reference for comparison. In this PWM, the duty ratio assigned to each space vector is equally shared in every switching cycle by all associated switching states. While the use of the conventional NTV PWM leads to the collapse of some capacitor voltages, the proposed VV PWM maintains balanced dc-link capacitor voltage operation. Additionally, the peak-to-peak value of the capacitor voltage ripple is inversely proportional to the switching (or carrier) frequency. Hence, for a given capacitor voltage ripple specification, the required capacitance can be reduced by increasing the switching frequency.

Let us compare the proposed \( n \)-level diode-clamped converter connected to a single dc-bus and operated with a VV PWM (design A) to two alternative converter designs based on the same topology. The first alternative design (design B) consists on a \( n \)-level diode-clamped converter with regulated dc voltage sources replacing the dc-link capacitors and operated with the NTV PWM described above. The second alternative design (design C) corresponds to a two-level converter operated with a conventional space vector modulation using the two possible switching states available for the zero vector in every switching cycle.

A. Component Count

From the point of view of component count, design C presents the minimum number of components, as it uses a simple two-level converter. Design A presents fewer components than design B, since it does not require the addition of regulated dc voltage sources replacing the dc-link capacitors. These sources can be implemented with \( n \)-level output-voltage regulated dc power supplies drawing the energy from the dc bus or through the introduction of specific PWM balancing circuits [13], [14].

B. Modulation Algorithm Computation Time

From the point of view of computation time required by the modulation algorithm, designs A and C are clearly superior to design B. For instance, the computation of 10000 line cycles with \( f_s / f_m = 100 \) (where \( f_m \) is the output fundamental frequency), \( m = 0.75 \), in a personal computer with an Intel Pentium D processor at 3 GHz, 1 GB of RAM, and using MATLAB 7.2, takes 1.45 s for design C. The computation time for design A is slightly higher (1.53 s for \( n = 3, 1.61 \) s for \( n = 4, \) and 1.66 s for \( n = 5 \)) and the computation time for design B is significantly higher (40.66 s for \( n = 3, 49.09 \) s for \( n = 4, \) and 55.75 s for \( n = 5 \)).

C. Total Harmonic Distortion

Fig. 8 shows the total harmonic distortion (THD) in the line-to-line output voltage of all three designs, as a function of the modulation index. Design B is clearly superior to A and C, particularly as the number of levels \( n \) increases. Design A is clearly superior to design C. The THD of designs A and B is the same for low modulation index values. As the modulation index increases, design A presents a progressively higher THD than design B and reaches the level of design C for \( m = 1 \).
D. Semiconductor Device Losses

A discussion follows regarding the comparison of semiconductor device losses in the main converter of all three designs. The comparison is made for the same dc-link voltage $V_{dc}$, the same output power, sinusoidal and balanced three-phase currents, negligible ac-side current ripple, unity displacement factor, and the same carrier frequency $f_s$.

Assuming a similar value of the conduction voltage drop per rated voltage for all semiconductor devices, conduction losses should be similar in all three designs. The main differences in device losses will be due to the different switching pattern. For each converter leg, switching transitions occur in pairs: one switch turns-off and one-switch turns-on. To simplify the analysis, it is assumed that diodes are ideal (lossless) and that the losses are concentrated either in the controlled device turning on or the device turning off, according to the pattern described in Fig. 9, where $v_i(t)$ and $i_i(t)$ are the voltage across the switch and the current through the switch, respectively. The absolute values of the voltage and current slopes during transitions are assumed to be constant and equal to 2$s_i$ and 2$s_i$, regardless of the value of $V_i$ and $I_i$. With these assumptions, the energy lost in a switching transition of an $n$-level converter leg is

$$E_i = \frac{V_{dc}^2 \cdot I_i}{2 \cdot (n-1)} \cdot s_i + \frac{V_{dc}^2 \cdot I_i^2}{2 \cdot (n-1)} \cdot s_i.$$  \hspace{1cm} (14)

Let us additionally assume that $s_i/s_i = V_{dc}/I_{pk}$, where $I_{pk}$ is the peak value of the phase current; i.e., the voltage and current transition times ($T_v$ and $T_i$) are equal for $V_{dc} = V_{dc}$ and $I = I_{pk}$. Fig. 10 shows the ratio of the switching losses in designs A ($P_{sA}$) and B ($P_{sB}$) with regard to the switching losses in design C ($P_{sC}$), for $n = 3, 4$ and 5. It can be observed that both designs A and B produce lower switching losses than design C. Design B is clearly the optimum, particularly for high modulation indices and number of levels. This means that design B produces lower switching losses in the multilevel converter than design A. However, from the point of view of the whole design losses, for a fair comparison, the losses in the regulated dc voltage sources replacing the dc-link capacitors must be considered in design B, which will probably lead to a higher total loss than in design A, since these regulated dc voltage sources process most of the energy flowing in between the dc-link and the ac side.

Fig. 11 shows the ratio $P_{sA}/P_{sC}$ as a function of the converter number of levels. This ratio depends on the total amount of switched voltage in design A [equal to $V_{dc}^2(3n–5)/(n–1)$ for $n \geq 3$] and the ratio $s_i/s_i$. As $n$ increases, $P_{sA}/P_{sC}$ tends to settle at a given value because the addition of all switching losses in design A occurring within $T_v$ tends to zero while the addition of all switching losses occurring within $T_i$ remains constant. This asymptotical value depends on the ratio $s_i/s_i$. As the ratio $s_i/s_i$ decreases, the proportion of the switching losses occurring during the current transitions decreases, and the asymptotical value of the ratio $P_{sA}/P_{sC}$ also decreases.
IV. EXPERIMENTAL RESULTS

Experimental tests have been conducted to verify the performance observed in Fig. 7 for a five level three-leg converter. A prototype built with 150 V metal oxide semiconductor field effect transistors (MOSFETs) has been used for this purpose. The converter is operated in inverter mode and open loop, with a dc power supply connected between dc-link points 1 and 5 and a three-phase series R-L load connected to the ac side. The computation of the twelve independent phase duty-ratios is performed by the embedded PowerPC of dSpace DS1103. This information is sent to an Altera EPF10K70 programmable logic device in charge of generating the twenty-four switch control signals.

Fig. 12 shows that the NTV PWM used as a reference for comparison leads to the collapse of the middle capacitor voltages $v_{C2}$ and $v_{C3}$. The same would occur with any other NTV PWM. On the other hand, with the proposed VV PWM all four capacitor voltages are fairly balanced in the absence of a closed-loop control. This control, however, is necessary in a real application to guarantee the balance under unequal switching behavior, leakage currents, etc. [21].

V. CONCLUSION

The definition of VVs guaranteeing the capacitor voltage balance even under non-linear loading conditions can be extended to any multilevel diode-clamped converter. This paper has presented the definition of these vectors for an $n$-level three-leg diode-clamped converter, and guidelines for designing practical VV PWMs. These guidelines take into consideration the number of switching transitions, the output-voltage distortion, and the simplicity of the final implementation.

The phase duty-ratio expressions that allow a simple implementation of these PWMs have also been presented for three- and two-leg converters. These PWMs (patent pending) guarantee capacitor voltage balance even for high modulation indexes, enabling the use of multilevel diode-clamped converters with passive front-ends.

The performance of an $n$-level three-leg diode-clamped converter operated with a VV PWM (design A) has been compared to the performance of two alternative designs: an $n$-level three-leg diode-clamped converter replacing the dc-link capacitors with regulated dc voltage sources and operated with a conventional NTV PWM (design B), and a two level converter operated with a conventional space vector modulation (design C). Table I presents their ranking in terms of different performance items.

Designs A and B offer a good alternative to design C because of their superior performance in terms of output-voltage harmonic distortion and converter losses, as expected. In applications with no stringent filtering requirements, design A might be the best solution, since it will probably present a lower total component cost and higher overall efficiency than design B.

![Fig. 12. Experimental results for $v_{C1}$, $v_{C2}$, $v_{C3}$, $v_{C4}$, $v_{ab}$, $i_a$, $i_b$, and $i_c$ in the following conditions: $V_{dc} = 120$ V, $m = 0.75$, $C = 155$ µF, $f_s = 5$ kHz, a linear and balanced load with per-phase impedance $Z_L = 33.5$ Ω $\angle 8.5^\circ$ (series R-L load), and a prototype using 150 V MOSFETs.](image)

(a) Reference NTV PWM. (b) Proposed VV PWM.
Therefore, VV PWMs lead to a competitive design solution that may allow highly integrated and compact converter designs based on diode-clamped topologies.

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<table>
<thead>
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<th>Feature</th>
<th>Design A</th>
<th>Design B</th>
<th>Design C</th>
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**TABLE I**

DESIGN RANKING

Key: 1-Best, 2-Middle, 3-Worst.

**REFERENCES**


