Diode-Clamped Multilevel Converters with Integrable Gate-Driver Power-Supply Circuits

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Keywords

«Multilevel converters», «Pulse Width Modulation (PWM)», «Modulation strategy», «Monolithic power integration», «System integration».

Abstract

Recent contributions in pulse width modulations (PWM) for multilevel diode-clamped converters enable the use of these converters with passive front-ends, any number of levels, and small dc-link capacitors. Highly compact converters designs based on these topologies can be envisioned. However, the design of the gate-driver power-supply for the multiple controlled semiconductor devices remains an important issue to be addressed. This paper focuses on the design of such circuits and the analysis of the resulting multilevel converter performance. A simple circuit connected across each power switch and monolithically integrable within it is selected. These circuits lead to simple, compact, and efficient converter designs. The main issues arising from the operation of the multilevel converter with such circuits are analyzed, and both hardware and software solutions are proposed. In particular, a new PWM strategy is presented. Experimental results are provided verifying the good performance of all proposed solutions.

Introduction

Multilevel converters have opened a door for advances in the electric energy conversion technology [1], [2], not only in high power applications, but also for medium and low power designs [3]–[5], since they present the advantages of a lower device voltage rating, a lower harmonic distortion, and higher efficiency compared to conventional two-level converters. This paper focuses primarily on medium and low power applications.

Among multilevel topologies, diode-clamped converters are especially interesting because of their simplicity (see Fig. 1). The multiple voltage levels are obtained through a series connection of identical capacitors. Recent contributions in PWMs for diode-clamped converters [6] have enabled the use of these converters with passive front-ends, any number of levels and small dc-link capacitors. This opens the

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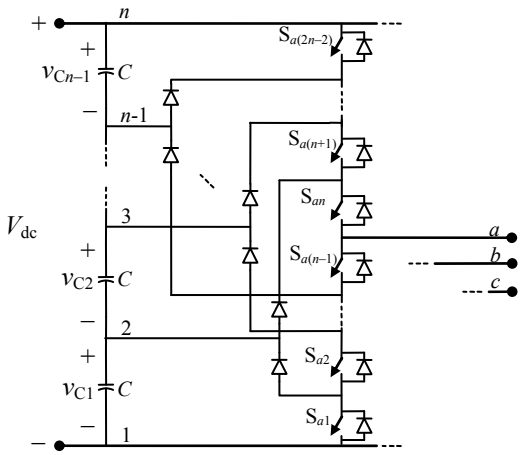

Fig. 1: *n*-level diode-clamped topology with multiple legs.

possibility of obtaining compact converter designs based on these topologies. However, in order to achieve a simple and integrable converter design, one of the first and most important issues to address is the design of the multiple isolated gate-driver power supplies required.

There are several options to generate an isolated low regulated voltage to feed the active-devices gate drivers: low-power dc-dc converters with galvanic isolation, topologies using coreless transformers, charge pump circuits, etc. Fig. 2 shows three possible structures. Fig. 2(a) presents a solution based on dc-dc converters with galvanic isolation extracting the energy from the dc-link capacitors. Every dc-link capacitor feeds two gate drivers. The two dc-dc converter outputs are isolated. Capacitor C_{sxi} stores the energy necessary to drive device S_{xi}. This structure has the benefits of an equally distributed energy withdrawal from the dc-link capacitors. The problem is the need for galvanic isolation for all dc-dc converters, which usually calls for the introduction of high-frequency transformers. This solution is therefore discarded because of its complexity, size and cost. An alternative solution without the need of galvanic isolation is shown in Fig. 2(b). This structure is based on the bootstrap charge pump concept, which has been already applied in multilevel converters [3], [5]. The single low-voltage power supply required by the structure can be obtained from the dc-link capacitor C_1, as shown in Fig. 2(b). However, these topologies are not adequate to be monolithically integrated within the active devices [7], can cause electromagnetic interference problems, and are asymmetric from both the point of view of topology and operation. Recently, other alternative topologies connected across the power device and being fully integrable within it have been proposed [7]–[10]. From these topologies, the structure in Fig. 2(c) is proposed. The gate-driver power-supply capacitors are fed from the energy available across the switch when it turns off. There are several options to implement the voltage regulator modules in Fig. 2(c) [7]–[10]. These circuits have been tested in simple buck and flyback dc-dc converters. This paper explores whether this concept can be applicable to a multilevel diode-clamped converter and evaluates the performance of such converters.

Gate-Driver Power-Supply Topology and Operation Principle

The selected gate-driver power-supply topology is shown in Fig. 3 [8]. The energy to drive the device is obtained from the energy that is otherwise lost during the main power switch S turn-off transition and, eventually, from the corresponding dc-link capacitor connected across the switch during its off state. This energy is stored in capacitor C_s. The current charging capacitor C_s flows through the auxiliary metal oxide semiconductor field effect transistor (MOSFET) S_a. The zener diode D_z, polarized by resistor R, limits the value of v_{Cs} and the blocking diode D_b prevents the discharging of C_s when the main power switch S is on.

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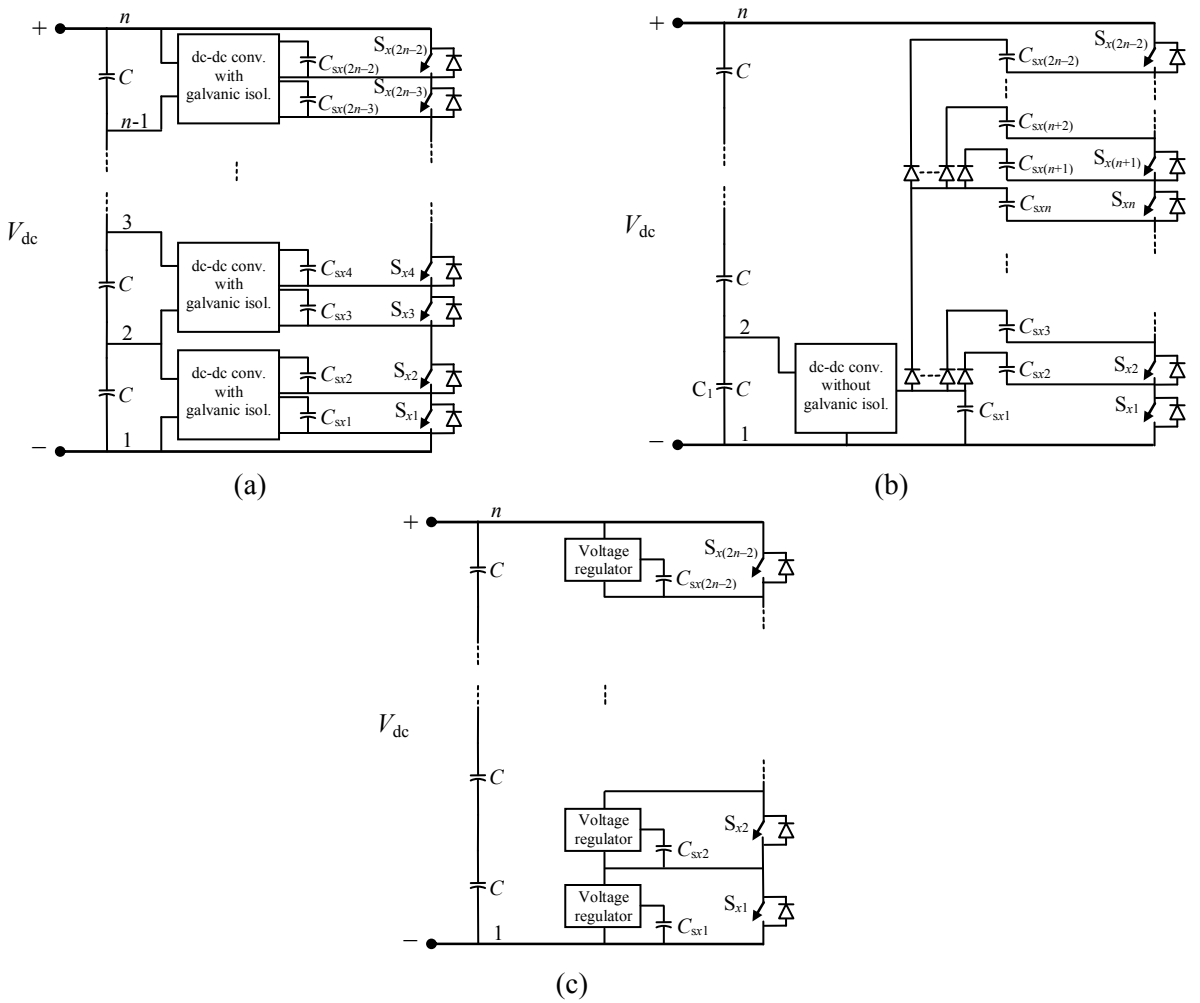

Fig. 2: Gate-driver power-supply structures for converter leg $x \in \{a, b, c\}$ (clamping diodes omitted). (a) Structure 1 based on dc-dc converters with galvanic isolation. (b) Structure 2 based on the bootstrap technique. (c) Structure 3 using voltage regulators connected across the active devices.

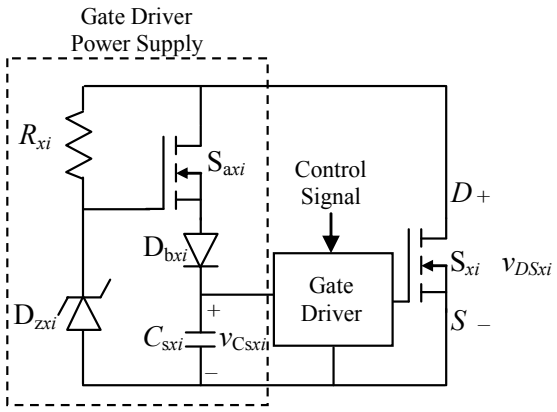

Fig. 3: Gate-driver power-supply circuit ($x \in \{a, b, c\}$, $i \in \{1, 2, \ldots, 2n-2\}$).

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Initial Converter Control

Adjustment of the Gate-Driver Power-Supply Capacity

To operate the converter, the PWM strategy presented in [6] and the capacitor-voltage balancing control presented in [11] are initially selected. This control scheme presents the benefit of guaranteeing the dc-link capacitor voltage balance in every switching cycle provided that the addition of the output leg currents equals zero, and thus, enables the operation of an n-level converter with low dc-link capacitance values. Fig. 4(a) presents the corresponding leg duty-ratio pattern (d_{xy}, corresponding to the leg x duty ratio of connection to dc-link point y) for a three-leg converter at a given modulation index value ($m \in [0,1]$ for linear modulation) over a line cycle (θ: ac-side line-cycle angle). The different power switch duty-ratios, d_{Sxi}, can be easily computed from these waveforms. It is important to note that the two most inner devices of each converter leg (S_{xn} and $S_{x(n-1)}$) remain on for 120º intervals every line cycle since the corresponding duty-cycle values

$$d_{Sx(n-1)} = \sum_{j=1}^{n-1} d_{xj} \qquad d_{Sxn} = \sum_{j=2}^{n} d_{xj} \tag{1}$$

are equal to the unity during these intervals. This prevents the corresponding capacitor C_s from being charged during this period. In order to prevent its discharging below the minimum voltage value for correct operation of the gate driver, it is required to select a capacitance value C_s higher than for other devices, for which the switch duty-ratio is always lower than the unity and, therefore, the corresponding capacitor C_s is recharged every switching cycle. This required value of C_{sxn} and $C_{sx(n-1)}$ will depend upon the ac-side line-cycle frequency (f_o). The lower the frequency is, the higher the required value of these two capacitors per leg.

The performance of this control scheme has been tested in the three-level three-leg converter prototype shown in Fig. 5. The components of the gate-driver power-supply are outlined in Table I. The converter is operated in inverter mode with a single dc power supply connected to dc-link points 1 and 3 and a wye-connected three-phase series R-L load connected to the ac side. The computation of the six independent phase duty-ratios is performed by the embedded PowerPC of dSpace DS1103. This information is sent to an Altera EPF10K70 programmable logic device in charge of generating the twelve switch control signals.

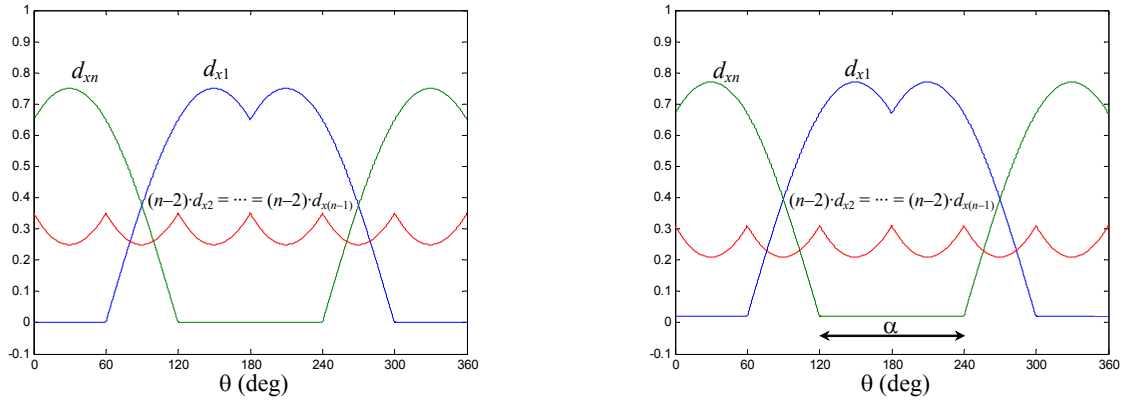

Fig. 4: Leg x duty-ratio pattern for an n-level three-leg converter (m = 0.75). (a) Original PWM scheme. (b) Modified PWM scheme with d_{offset} = 0.02.

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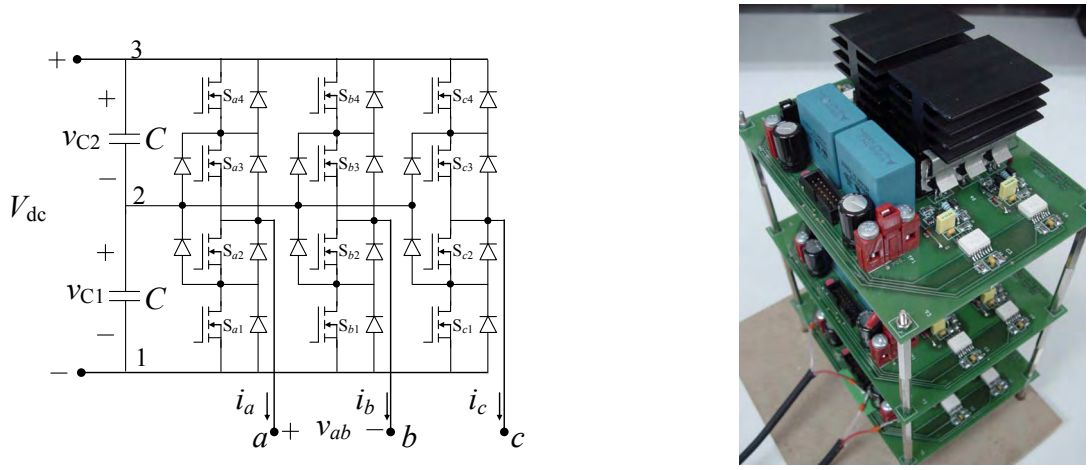

(a) (b)

Fig. 5: Three-level three-leg dc-ac converter. (a) Topology. (b) Prototype using 150 V MOSFETs as devices S_{xi}.

Table I: Gate-driver power-supply components

Component Symbol	Selected Component
S_a	IRF5802TR (150 V, 0.9 A)
D_b	10BQ040 (40 V, 1 A)
R	10 kΩ
D_z	BZX85C22 (22 V)
C_s	330 nF, polypropilene

Fig. 6 shows the experimental results obtained with this control scheme and adding 10 μF electrolytic capacitors to C_{sx2} and C_{sx3}. It can be observed that the converter is operating correctly at a high modulation index value (m = 0.95). Note the footprint of the selected PWM on the line-to-line voltage v_{ab}. We can also observe that during a 120º period over the line cycle, capacitor C_{sa2} discharges because the corresponding device is on. However, the addition of 10 μF capacitors to these inner switch positions prevents the supply voltage from falling beyond the minimum allowed value. Once the device starts switching on and off in every switching cycle, the capacitor is quickly recharged. As mentioned earlier, the value of the required capacitance depends on the output line-cycle frequency. Typically, a relatively high value will be needed, which implies that the recharging process will take place essentially during the off state of the main device without recycling turn-off losses and therefore presenting a lower efficiency.

Addition of an Auxiliary Bootstrap Circuit

An alternative solution to increasing the value of C_s for the two most inner devices of each leg is the introduction of two diodes per leg to implement the bootstrap circuit of Fig. 7. This bootstrap circuit involves three power devices per leg: S_{xn}, $S_{x(n-1)}$, and $S_{x(n-2)}$. During the 120º in which $S_{x(n-1)}$ is on, its corresponding gate-driver power-supply capacitor is fed from the energy stored in $C_{sx(n-2)}$. During the 120º in which S_{xn} is on, its corresponding gate-driver power-supply capacitor is fed from the energy stored in $C_{sx(n-1)}$.

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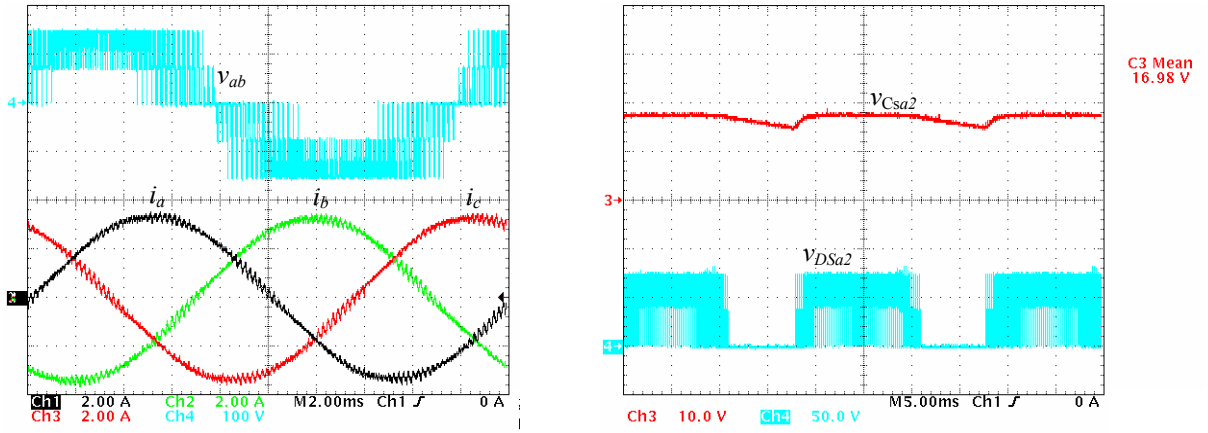

Fig. 6: Experimental results for v_{ab}, i_a, i_b, i_c, v_{Csa2}, and v_{DSa2} in the following conditions: V_{dc} = 150 V, m = 0.95, C = 155 µF, $C_{sx1} = C_{sx4}$ = 330 nF, $C_{sx2} = C_{sx3}$ = 330 nF + 10 µF ($x \in \{a, b, c\}$), switching or carrier frequency f_s = 5 kHz, and a linear and balanced load with per-phase impedance Z_L = 22.5 Ω ∠12º (series R-L load).

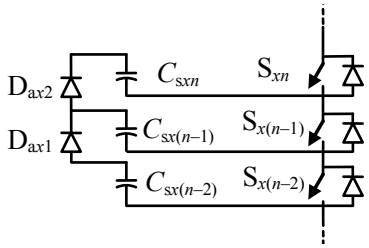

Fig. 7: Auxiliary bootstrap circuit.

Fig. 8 shows the experimental results of this new configuration with the three-level converter prototype of Fig. 5 and all gate-driver capacitors equal to 330 nF. The converter is operating correctly. However, note the voltage drop in v_{Csa2} and v_{Csa3} due to the conduction voltage drop in the auxiliary diodes D_{aa1} and D_{aa2}. Additionally, these two extra diodes per leg cannot be monolithically integrated within the power devices.

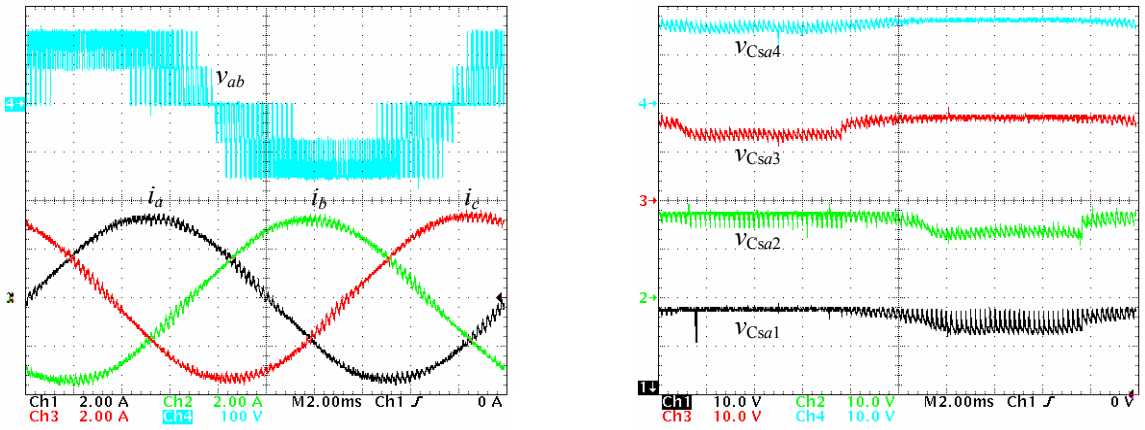

Fig. 8: Experimental results for v_{ab}, i_a, i_b, i_c, v_{Csa1}, v_{Csa2}, v_{Csa3}, and v_{Csa4} in the following conditions: V_{dc} = 150 V, m = 0.95, C = 155 µF, $C_{sx1} = C_{sx2} = C_{sx3} = C_{sx4}$ = 330 nF ($x \in \{a, b, c\}$), auxiliary diodes D_{ax1} and D_{ax2} 1N4148, switching or carrier frequency f_s = 5 kHz, and a linear and balanced load with per-phase impedance Z_L = 22.5 Ω ∠12º (series R-L load).

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Modified Converter Control

The previous converter control scheme performs satisfactorily, but requires an increased value of C_s for the two most inner devices of each leg or the addition of two diodes per leg to implement the auxiliary bootstrap circuit of Fig. 7. In order to be able to operate with the configuration of Fig. 2(c), with the same low C_s value for all devices, and without the need of extra diodes, therefore obtaining a simple modular design, a new PWM strategy is proposed modifying the previous one. The equations describing this new PWM scheme with reference to the original [6] are

$$\begin{aligned} d'_{x1} &= d_{x1} + d_{\text{offset}} \\ d'_{xn} &= d_{xn} + d_{\text{offset}} \\ d'_{xi} &= d_{xi} - \frac{2 \cdot d_{\text{offset}}}{n-2} \\ x &\in \{a,b,c\}; \quad i \in \{2,3,...,n-1\} \end{aligned} \tag{2}$$

where d_{offset} is given, in principle, a small constant value over time. Fig. 4(b) presents the leg duty-ratio pattern for $d_{\text{offset}} = 0.02$. It can be seen that the original duty-ratio waveforms d_{x1} and d_{xn} are slightly shifted upwards, so that both leg duty-ratios are always greater than zero. This is equivalent to employing switching states 111 and *nnn* in approximating the reference vector when defining the PWM strategy with the aid of a space vector diagram [6]. This modification does not affect the switching-frequency averaged voltage waveforms since a zero average offset is applied to the three converter leg voltages v_{x1}.

The proposed PWM strategy has been tested in the prototype of Fig. 5 with C_s = 330 nF for all gate-driver power-supply capacitors. Fig. 9 and Fig. 10 present the experimental results. It can be observed that the converter is performing satisfactorily for both high (Fig. 9(a)) and low (Fig. 9(b)) modulation index values. Note the new footprint of the PWM scheme on the line-to-line voltage v_{ab} and that the dc-link capacitor voltages v_{C1} and v_{C2} are balanced in every switching cycle. Fig. 10 shows the gate-driver power-supply capacitor voltages and drain-to-source voltages of devices S_{a2} and S_{a4} (see Fig. 5(a)). A few switching periods are shown corresponding to the 120º region α in Fig. 4(b). Capacitor C_{sa2} is correctly recharged every switching cycle despite the short period of time device S_{a2} is off.

The new PWM scheme allows operating with the gate-driver power-supply structure of Fig. 2(c) and small C_s capacitors regardless of the output line-cycle frequency. However, this advantage is obtained at the expense of increasing the number of switching transitions per switching cycle (and hence, the switching losses), increasing the ac-side voltage harmonic distortion, and reducing the maximum value of the modulation index in the linear modulation range.

First of all, the percentage increase in per-switching-cycle switching transitions of the modified PWM strategy with reference to the original PWM strategy is

$$\Delta st = \frac{2}{3n-5} \cdot 100 \quad (\%), \tag{3}$$

Fig. 11 deploys this percentage increase as a function of the number of levels. It can be seen that Δst decreases rapidly as the number of levels increases, and so does the associated increase in switching losses. Therefore, for a value of n large enough the increase in switching losses might be deemed not significant.

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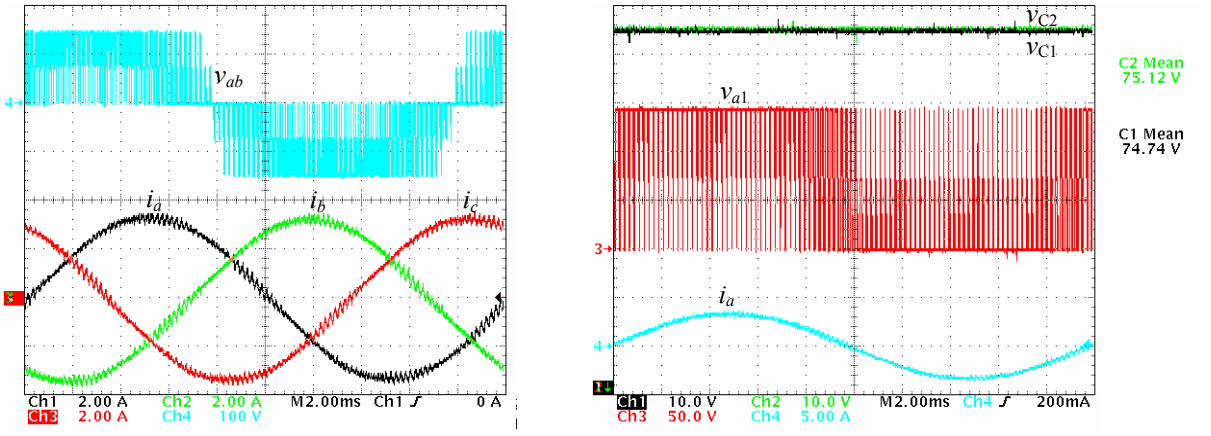
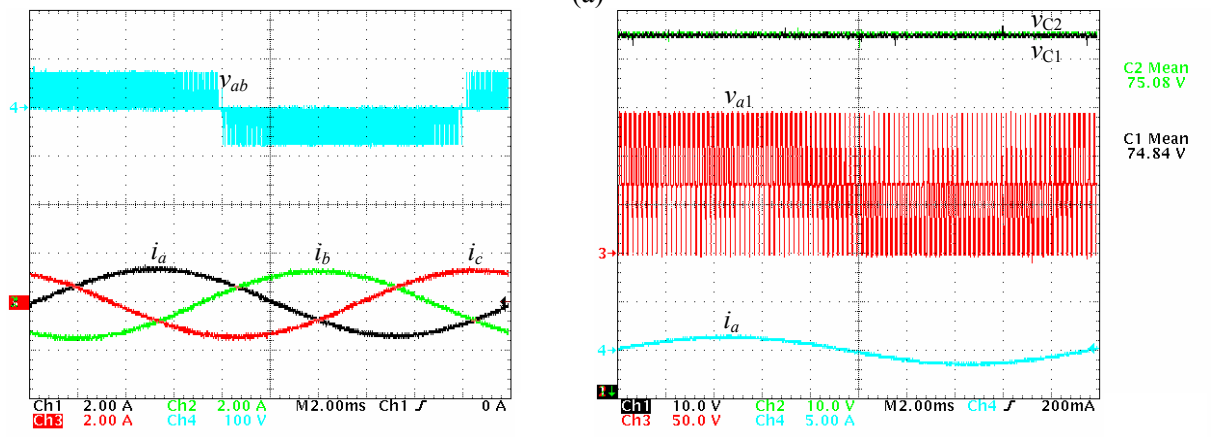


(a)



(b)

Fig. 9: Experimental results for v_{ab}, i_a, i_b, i_c, v_{C1}, v_{C2}, and v_{a1} in the following conditions: V_{dc} = 150 V, C = 155 µF, $C_{sx1} = C_{sx2} = C_{sx3} = C_{sx4}$ = 330 nF ($x \in \{a, b, c\}$), d_{offset} = 0.02, f_s = 5 kHz, and a linear and balanced load with per-phase impedance Z_L = 22.5 Ω ∠12º (series R-L load). (a) m = 0.95. (b) m = 0.4.

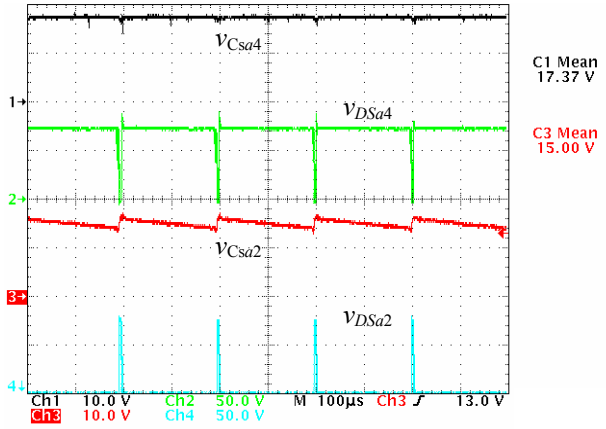


Fig. 10: Experimental results for v_{Csa2}, v_{Csa4}, v_{DSa2}, and v_{DSa4} in the same conditions as in Fig. 9 and m = 0.95.

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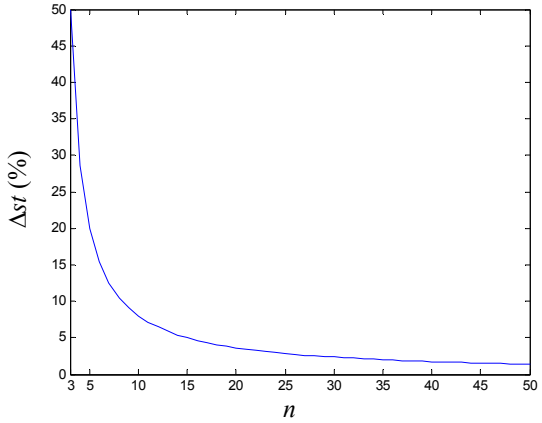

Fig. 11: Percentage increase in per-switching-cycle switching transitions of the modified PWM strategy with reference to the original PWM strategy, as a function of the number of levels.

Second, Fig. 12 presents the total harmonic distortion (*THD*) in the output line-to-line voltage of a five-level three-leg diode-clamped converter as a function of the modulation index for both the original and modified PWM schemes. It can be observed that there is a clear increase of the *THD* in the new PWM strategy, especially for high values of m. However, this increase may not be significant for many applications.

Finally, since all duty-ratios must have a value between 0 and 1, the maximum value of the modulation index in the linear modulation range with the modified PWM strategy is

$$m_{\max} = 1 - 2 \cdot d_{\text{offset}} \tag{4}$$

In general, this decrease in the maximum value is not significant since a small value of d_{offset} can be typically selected. The minimum value of d_{offset} is determined from the driver and device technology.

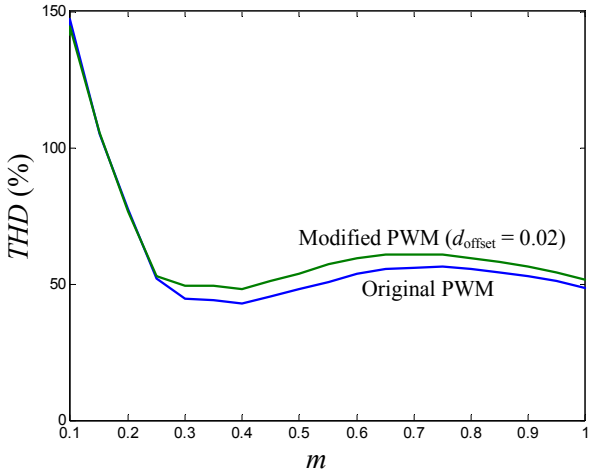

Fig. 12: *THD* in the line-to-line voltage of a five-level three-leg diode-clamped converter as a function of the modulation index m. Conditions: $f_s / f_o = 100$ and harmonics considered up to $40 \cdot f_s$.

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Conclusion

This paper proves the feasibility of integrating the gate-driver power supply in all devices of a multilevel diode-clamped converter. These transformerless circuits avoid the need of incorporating conventional isolated dc-dc power supplies to feed each device driver and, hence, lead to simple and compact multilevel converter designs, more efficient than conventional two-level converters.

The use of existing PWM strategies for operating the multilevel converter requires an increase of two gate-driver power-supply capacitances per leg or the introduction of two bootstrap diodes per leg. Alternatively, the novel PWM strategy presented can be used in order to achieve a simple modular design, independent from the output ac voltage frequency and without the need of additional components. This solution combines the benefits of being modular and integrable, and ensures that the energy required to drive the switches is drawn homogenously from all dc-link capacitors. The drawbacks from this new PWM with regard to switching losses are not significant for a number of levels large enough. The increase in ac-side voltage distortion and the decrease in maximum modulation index may not be significant for many applications.

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