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A new high-efficiency single-phase transformerless PV inverter topology

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ABSTRACT: There is a strong trend in the photovoltaic (PV) inverter technology to use transformerless topologies in order to acquire higher efficiencies combining with very low ground leakage current. In this paper a new topology, based on the H-Bridge with a new AC bypass circuit consisting in a diode rectifier and a switch with clamping to the DC midpoint is proposed. The topology is simulated and experimentally validated and a comparison with other existing topologies is performed. High conversion efficiency and low leakage current is demonstrated.

I INTRODUCTION

Photovoltaic inverters become more and more widespread within both private and commercial circles. These grid connected inverters convert the available direct current supplied by the photovoltaic (PV) panels and feed it into the utility grid. According to the latest report on installed PV power, during 2007 there has been a total of 2.25GW of installed PV systems, out of which the majority (90%) has been installed in Germany, Spain, USA and Japan. At the end of 2007 the total installed PV capacity has reached 7.9 GW of which around 92% is grid connected [1].

There are two main topology groups used in case of grid connected PV systems and they are: with and without galvanic isolation [2]. Galvanic isolation can be on the DC side, in the form of a high frequency DC-DC transformer or on the grid side in the form of a big-bulky AC transformer. Both of these solutions offer the safety and advantage of galvanic isolation, but the efficiency of the whole system is decreased, due to power losses in these extra components. In case the transformer is omitted the efficiency of the whole PV system can be increased with an extra 1-2%. The most important advantages of transformerless PV systems can be observed in Fig. 1, like: higher efficiency, smaller size and weight compared to the PV systems that have galvanic isolation (either on the DC or AC side).

Fig. 1 has been made from the database of more than 400 commercially available PV inverters, presented in a commercial magazine about PV systems [3]. Transformerless inverters are represented by the dots (Transformerless), while the triangles represent the inverters that have a low-frequency transformer on the grid side (LF-transformer) and last the stars represent the topologies including a high-frequency DC-DC transformer (HF-transformer), adding a galvanic isolation between the PV and grid. The conclusion drawn from these graphs is that transformerless inverters have higher efficiency, smaller weight and size than their counterparts with galvanic separation.

Transformerless PV inverters use different solutions to minimize the leakage ground current and improve the efficiency of the whole system, an issue that has previously been treated in many papers [4]-[11].

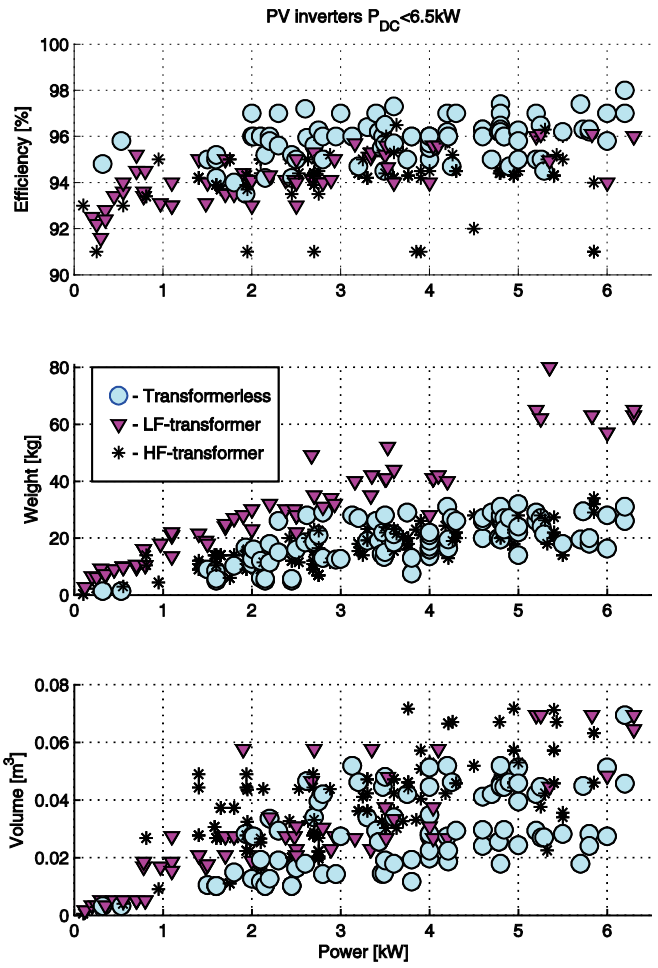

Fig. 1: Advantages and drawback of different inverter topologies

In order to minimize the ground leakage current through the parasitic capacitance of the PV array, several techniques have been used.

One of them is to connect the midpoint of the DC-link capacitors to the neutral of the grid, like the half-bridge, Neutral Point Clamped (NPC) or three-phase full bridge with a split capacitor topology, thereby continuously clamping the PV-array to the neutral connector of the utility grid. Half-bridge and NPC type of converters have very high efficiency, above 97%, as shown in [6]. Furthermore the topology proposed in [6] reduces the DC current injection, which is an important issue in case of transformerless topologies and is limited by different standards. The non injection of DC current into the grid is

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topologically guaranteed by adding a second capacitive divider to which the neutral terminal of the grid is connected. An extra control loop is introduced that compensates for any DC current injection, by controlling the voltage of both capacitive dividers to be equal. A disadvantage of half-bridge and NPC type of converters is that for single phase grid connection they need a 700V DC-link.

Another solution is to disconnect the PV-array from the grid, in case of H-Bridge (HB) inverters, when the zero vector is applied to the load (grid). This disconnection can be done either on the DC side of the inverter (like the topology from [4] and H5 topology from SMA [13]) or on the AC side (like the HERIC topology from Sunways[12])

In this paper a new topology called HB-ZVR (H-Bridge Zero Vector Rectifier) is proposed where the mid-point of the DC link is clamped to the inverter only during the Zero Vector period by means of a diode rectifier and 1 switch.

In section II a comparison of known transformerless topologies and the HB-ZVR is performed using simulation, focusing on the voltage to earth and ground leakage current. In section III experimental results are shown, confirming the simulations. Section IV presents the efficiency curve of the compared topologies.

II TRANSFORMERLESS TOPOLOGY ANALYSIS:

As discussed in previous works [8],[11] the common mode voltage generated by a topology and modulation strategy can greatly influence the ground leakage current that flows through the parasitic capacitance of the PV array. Generally the utility grid does not influence the common mode behavior of the system, so it can be concluded that the generated common mode voltage of a certain inverter topology and modulation strategy can be shown using a simple resistor as load. Therefore in case of the simulations only a resistive load is used and the common-mode voltage is measured between the DC+ terminal of the DC source and the grounded middle-point of the resistor as shown in Fig. 2.

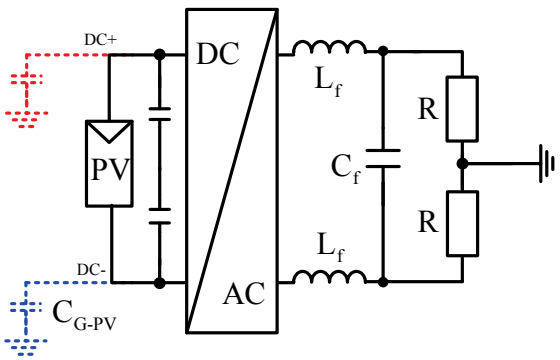

Fig. 2. Test setup used for common-mode voltage measurement

In the following simulation results obtained using Matlab Simulink with the PLECS toolbox are shown. The simulation step size is 0.1µs, with an 8kHz switching frequency.

Simulation parameters:

L_f=1.8mH, filter inductance
C_f=2µF, filter capacitor
R=7.5Ω, load resistance
V_{dc}=350V, input DC voltage
C_{dc}=250µF, DC-link capacitor
C_{G-PV}=100nF, parasitic capacitance of PV array
F_{sw}=8kHz, switching frequency for all cases except the switching frequency for unipolar PWM has been chosen to be F_{sw}=4kHz, so the output voltage of the inverter has the same frequency for all cases.

II.1 HB with unipolar switching

Most single-phase HB inverters use unipolar switching in order to improve the injected current quality of the inverter, which is done by modulating the output voltage to have three levels with twice the switching frequency. Moreover this type of modulation reduces the stress on the output filter and decreases the losses in the inverter.

The positive active vector is applied to the load by turning ON S1 and S4, as shown in Fig. 3.

The negative active vector is done similarly, but in this case S2-S3 is turned-ON.

In case of the unipolar switching pattern, the zero voltage state, during the positive voltage, is achieved by short circuiting the output of the inverter, as detailed in Fig. 4, which results in a high frequency content in the generated common-mode voltage.

As seen in Fig. 6, in case of a transformerless PV system using this type of topology and modulation, the high-frequency common-mode voltage, measured across C_{G-PV}, will lead to very high leakage ground current, making it unsafe, therefore not usable (recommended) for transformerless PV applications.

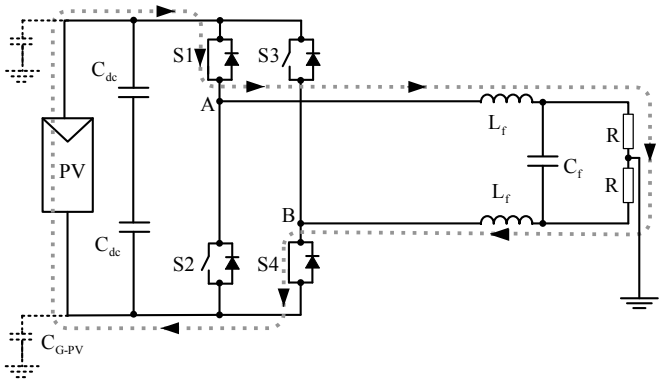

Fig. 3. HB-Unip topology, active vector applied to load, using S1-S4 for positive voltage

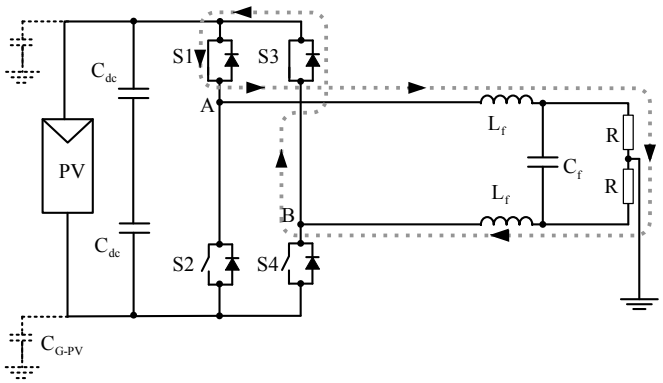

Fig. 4. HB-Unip topology, zero vector applied to load, using S1-S3 for positive voltage

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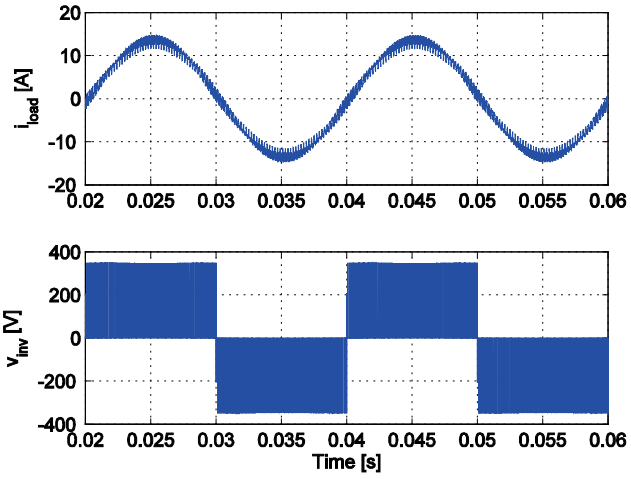

Fig. 5. HB-Unip topology, load current and inverter output voltage

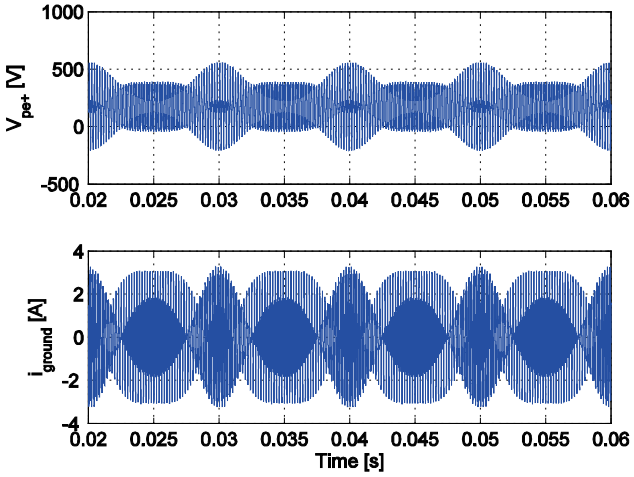

Fig. 6. HB-Unip topology, voltage to ground and ground leakage current

II.2 HERIC – Highly Efficient and Reliable Inverter Concept

This topology, shown in Fig. 7, combines the advantages of the three-level output voltage of the unipolar modulation with the reduced common-mode voltage, as in the case of bipolar modulation. This way the efficiency of the inverter is increased, without compromising the common-mode behavior of the whole system.

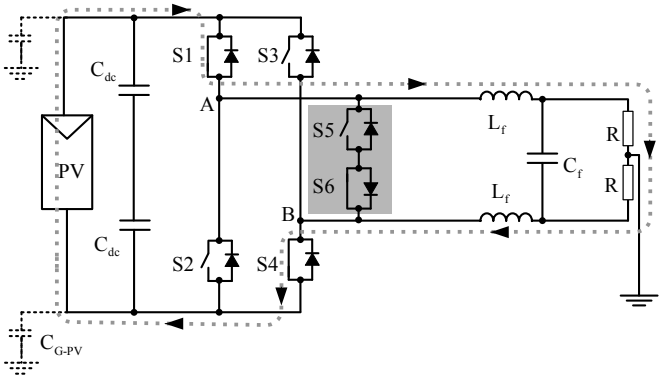

Fig. 7. HERIC topology, active vector applied to load, using S1-S4 during positive half-wave

The zero voltage vector is realized using a bidirectional switch shown with a grey background in Fig. 7. This bidirectional switch is made up of 2 IGBTs and 2 diodes (S5-S6). During the positive half-wave of the load (grid) voltage, S6 is switched ON and is used during the freewheeling period of S1 and S4. On the other hand, during the negative half-wave S5 is switched ON and is used during the freewheeling period of S2 and S3 [12].

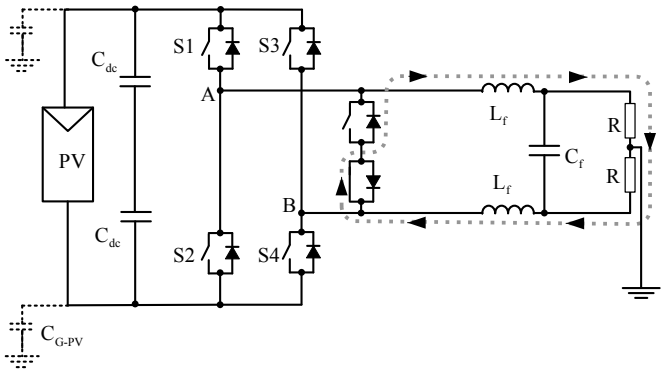

Fig. 8. HERIC topology, zero vector applied to load, using S6 during positive half-wave

This way, using S5 or S6 as detailed in Fig. 8, the zero voltage vector is realized by short-circuiting the output of the inverter, during which period the PV is separated from the grid, because S1-S4 or S2-S3 are turned OFF.

As shown in Fig. 9, the output voltage of the inverter has three levels and the load current ripple is very small, although in this case the frequency of the current is equal to the switching frequency. As seen in Fig. 10, the inverter generates no common-mode voltage therefore the leakage current through the parasitic capacitance of the PV would be very small.

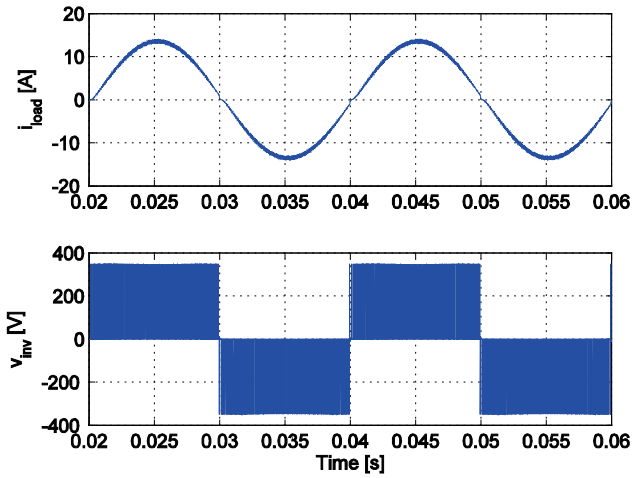

Fig. 9. HERIC topology, load current and inverter output voltage

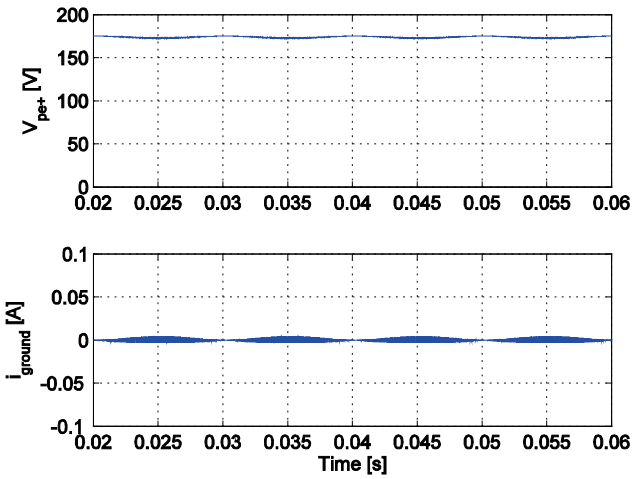

Fig. 10. HERIC topology, voltage to ground and ground leakage current

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II.3 Proposed topology (HB-ZVR)

Another solution for generating the zero voltage vector can be done using a bidirectional switch made of 1 IGBT and 1 diode bridge. The topology is detailed in Fig. 11, showing the bidirectional switch, as an auxiliary component with a grey background. This bidirectional switch is clamped to the midpoint of the DC-link capacitors in order to fix the potential of the PV array also during the zero voltage vector when S1-S4 and S2-S3 are open. An extra diode is used to protect from short-circuiting the lower DC-link capacitor.

During the positive half wave S1-S4 is used to generate the active vector, supplying a positive voltage to the load, as show in Fig. 11.

The zero voltage state is achieved by turning ON S5 when S1-S4 are turned OFF, as shown in Fig. 13. The gate signal for S5 will be the complementary gate signal of S1-S4, with a small deadtime to avoid short-circuiting the input capacitor. Using S5 it is possible for the grid current to flow in both directions, this way the inverter can feed also reactive power to the grid, if necessary.

During the negative half wave of the load voltage, S2-S3 are used to generate the active vector and S5 is controlled using the complementary signal of S2-S3 and generates the zero voltage state, by short-circuiting the outputs of the inverter and clamping them to the midpoint of the DC-link.

During the deadtime, between the active vector and the zero state, there is a short period while all the switches are turned OFF, when the freewheeling current finds its path through the antiparallel diodes to the input capacitor. This is shown in Fig. 12 and leads to higher losses, compared to the HERIC topology, where the freewheeling current finds its path through the bidirectional switch, either through S5 or S6, depending on the sign of the current.

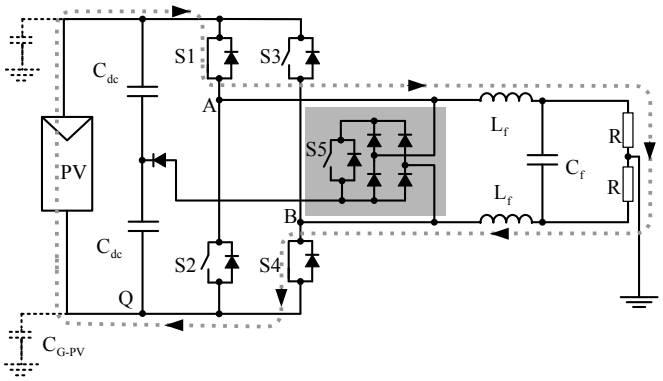

Fig. 11. HB-ZVR topology, active vector applied to load, using S1-S4, during positive half-wave

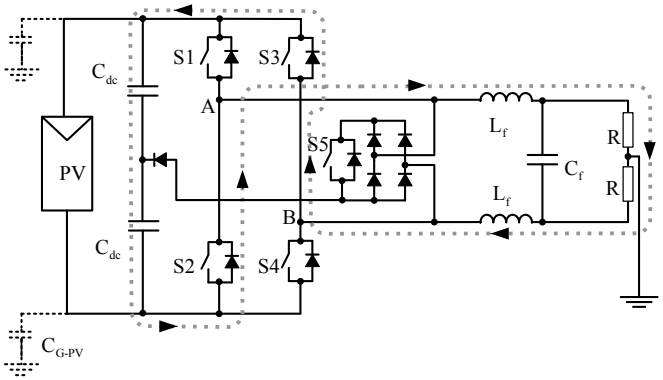

Fig. 12. HB-ZVR topology, dead-time between turn-OFF of S1-S4 and turn-ON of S5, during positive half-wave

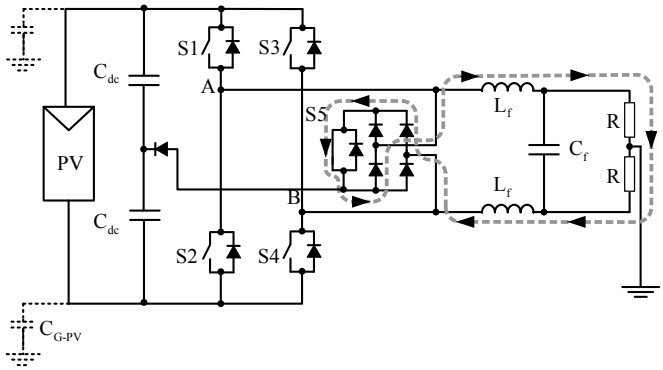

Fig. 13. HB-ZVR topology, zero vector applied to load, using S5, during positive half-wave

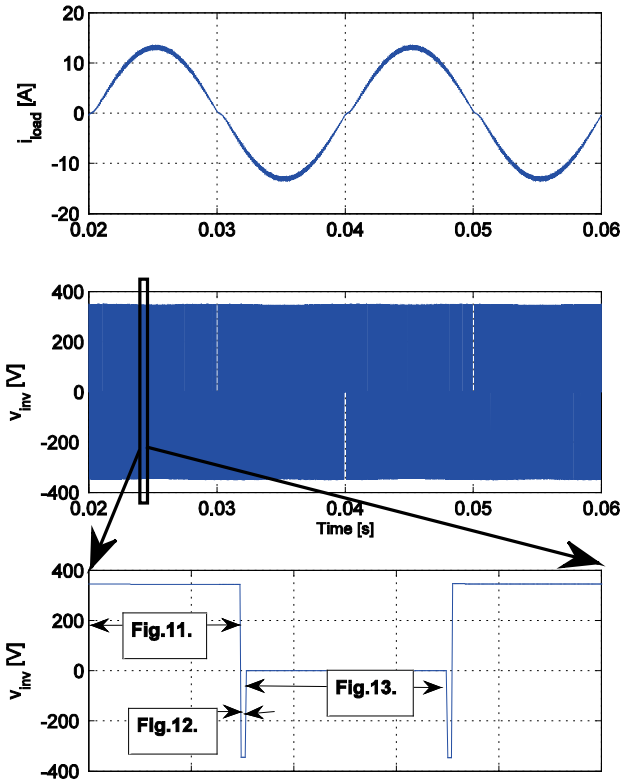

Fig. 14. HB-ZVR load current and inverter output voltage

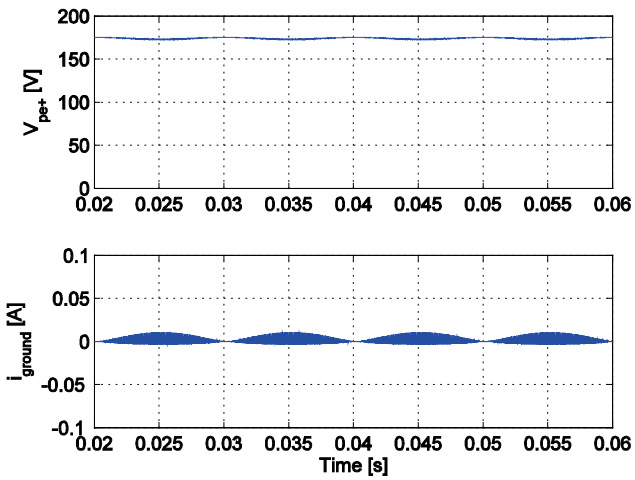

Fig. 15: HB-ZVR topology, voltage to ground and ground leakage current

As shown in Fig. 14, the output voltage of the inverter has three levels, taking into account the freewheeling part during deadtime. In this case also, the load current ripple

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is very small and the frequency is equal to the switching frequency.

To show that this topology does not generate a varying common-mode voltage, V_{cm} has been calculated for the switching states regarding the positive, zero and negative vectors:

$$V_{cm} = \frac{V_{AQ} + V_{BQ}}{2} \quad (1)$$

$$\text{Positive: } V_{AQ} = V_{dc};\ V_{BQ} = 0 \Rightarrow V_{cm} = \frac{V_{dc}}{2} \quad (2)$$

$$\text{Zero: } V_{AQ} = \frac{V_{dc}}{2};\ V_{BQ} = \frac{V_{dc}}{2} \Rightarrow V_{cm} = \frac{V_{dc}}{2} \quad (3)$$

$$\text{Negative: } V_{AQ} = 0;\ V_{BQ} = V_{dc} \Rightarrow V_{cm} = \frac{V_{dc}}{2} \quad (4)$$

As detailed by equations (1)-(4), the common-mode voltage is constant for all switching states of the converter. Therefore the leakage current through the parasitic capacitance of the PV would be very small, as observed in Fig. 15.

III EXPERIMENTAL RESULTS

In case of the experimental results, the setup has the same parameters as was the case of the simulations: V_{dc}=350V, C_{dc}=250µF, L_f=1.8mH, C_f=2µF, F_{sw}=8kHz, deadtime=2.5µs.

To compare the behavior of the different inverters, all three topologies have been tested using the same components. PM75DSA120 Intelligent Power Modules with maximum ratings of 1200V and 75A from Mitsubishi as IGBTs and DSEP 30-06BR with maximum ratings of 600V 30A as diodes from IXYS have been used in the diode bridge of the proposed topology.

The modular based setup shown in Fig. 16 makes it possible to test the different topologies, like: full-bridge with bipolar or unipolar modulation, the HERIC topology and the proposed HB-ZVR, using the same components.

III.1 HB with unipolar switching (experiment)

The main advantage of the HB inverter with unipolar switching is that the output voltage has three-levels and the frequency of the output voltage is the double of the switching frequency, thereby increasing the efficiency of the inverter and decreasing the size of the output filter. But the major drawback of this topology is the high frequency common-mode voltage, which makes it unsuitable to be used for transformerless PV systems.

As seen in Fig. 17, the unipolar PWM strategy used in case of the HB topology generates a high-frequency common mode voltage, measured between the DC+ terminal of the DC-link and ground, shown by channel 1 in Fig. 17.

As also shown in Fig. 17, the FFT represented by channel M, details the spectrum of the common mode voltage. This common-mode voltage has very high amplitudes both at DC and the switching frequency. Also a low frequency component can be seen on the measured voltage, which is caused by the 100Hz single-phase power variation.

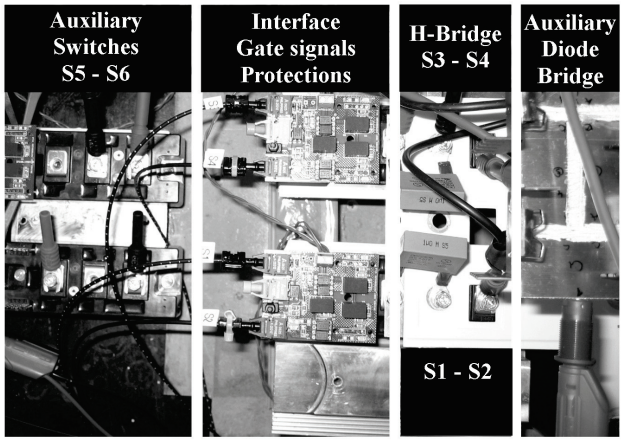

Fig. 16. Experimental setup, modular solution

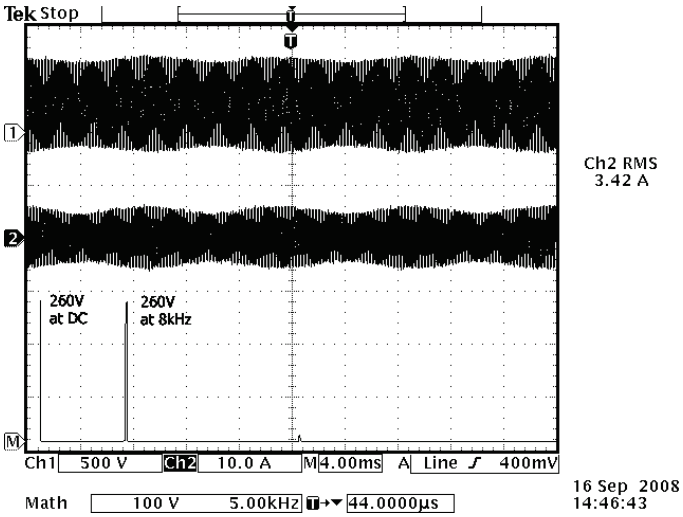

Fig. 17. Common-mode voltage (FFT) and ground current, FB-unipolar

This varying common-mode voltage generates a very high ground leakage current that is only limited by the parasitic capacitance of the PV array. In this case the leakage current reaches to peaks around 6A as shown by channel 2 in Fig. 17.

III.2 HERIC (experiment)

As presented in the simulation results (II.2), the HERIC topology generates a constant common-mode voltage, by disconnecting the PV from the load (grid) during the state of the zero vector, when the output of the inverter is short circuited. This separation assures, that the common-mode voltage acting on the parasitic capacitance of the PV array does not change in time, therefore keeping the leakage current at very low values, well below the standard requirement of 300mA, given by VDE-0126-1-1, the German standard for grid connected PV systems.

As shown in Fig. 18 the voltage measured between the DC+ terminal of the DC-link and ground is constant and has no high frequency content, represented by channel 1 on the scope. An FFT of channel 1 also shows only a DC component of the measured voltage.

Furthermore, the leakage current, represented by channel 2 in the scope results in Fig. 18, is also very low, with an RMS value around 22mA.

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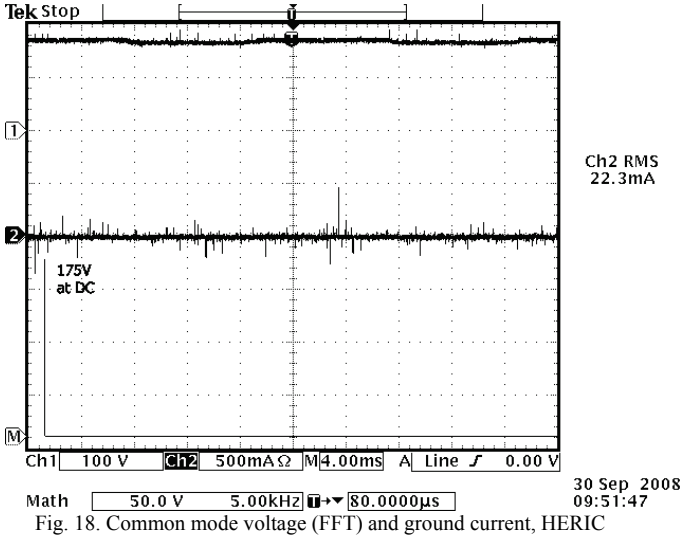

Fig. 18. Common mode voltage (FFT) and ground current, HERIC

III.3 HB-ZVR (experiment)

As mentioned in II.3 the HB-ZVR topology generates the zero voltage vector in a similar way as the HERIC topology, but using another solution for the bidirectional switch configuration. Of course the common-mode behavior of the topology is similar, as was the case of the HERIC topology.

As shown in Fig. 19 the voltage measured between the DC+ terminal of the DC-link and ground is constant and has no high frequency content, represented by channel 1 on the scope picture. An FFT of this voltage also shows only a DC component without any high frequency components.

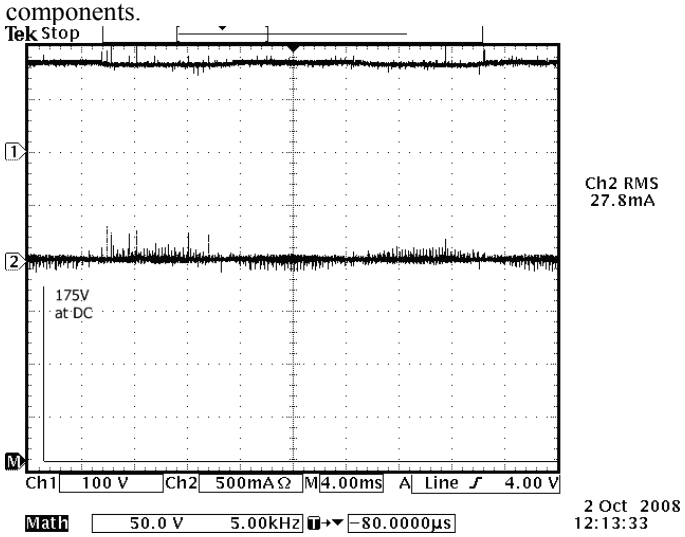

Fig. 19. Common mode voltage (FFT) and ground current, HB-ZVR

In this case also, as detailed by channel 2 in the scope results from Fig. 19, the leakage current, has also very low values, with an RMS value around 27mA.

IV EFFICIENCY

In case of a single-phase grid connection, the required minimum DC-link input voltage of the inverter, in the European case, has to be at least 350V, otherwise a boost stage is required. The tests have been done with an input voltage of V_{dc}=350V.

The HERIC topology, as also suggested by its name, has very high conversion efficiency throughout the whole working range and has the best efficiency within the compared topologies, as detailed in Table 1 and shown also in Fig. 20.

The HB-ZVR topology has a slightly lower efficiency, due to the fact that the bidirectional switch is controlled with the switching frequency, while in case of the HERIC topology, the bidirectional switch is only switched with the mains frequency. With a maximum efficiency of 94,88% it is a very attractive solution for transformerless PV systems.

The HB-Bip topology has the lowest efficiency, due to the high losses as a result of the two level voltage output.

The efficiency of the HB-Unip topology has not been included in the efficiency comparison of the transformerless topologies from Fig. 20 and Table 1, because of the influence of the galvanic isolation, where extra losses, as high as 2%, are possible due to the added transformer.

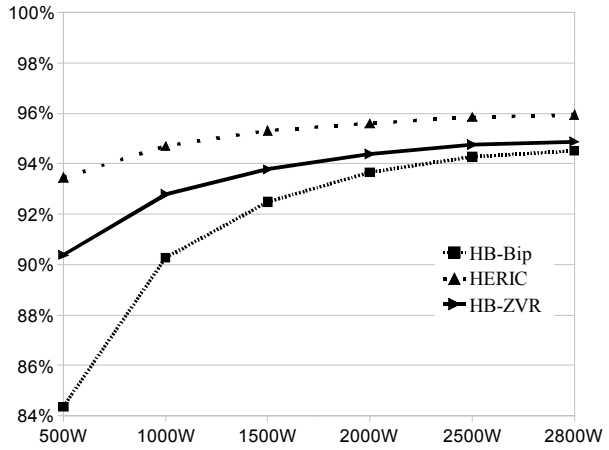

Fig. 20. Efficiency curve of the different topologies (V_{dc}=350V)

Nowadays most PV inverters are current controlled, injecting only active power into the utility grid. In case there are many inverters injecting active power at the same time, the voltage at Point of Common Coupling (PCC) might rise over the limits stated in the standards and trigger the safety of the inverters leading to disconnection or limit the power production below the available power. This leads to extra losses because not all the available PV power is fed into the grid. In case PV inverters would have a P-Q implemented control, the before mentioned drawback could be dealt with by injection of reactive power, thereby controlling the voltage at PCC. Therefore the capability of injecting reactive power would be a major advantage of future PV inverters, improving the total production of the PV system.

The advantage of HB-ZVR is that the HERIC topology, with the implemented PWM strategy, is only ideal for PV systems that supply the grid with active power, otherwise said to have the power factor: $\cos\varphi = 1$. This is because the bidirectional switch of the HERIC topology made up of S5 and S6 is not controlled to be turned-ON simultaneously, therefore current can only flow in a predefined direction, defined by the currently turned-ON switch.

On the other hand, in case of the HB-ZVR, it does not matter what the sign the load current has, it will always find a path through the bidirectional switch, made up of a diode bridge and a switch. This makes it possible to have a reactive power flow that can be used to support the utility

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grid with additional services any time during the functioning of the inverter.

Disadvantage of HB-ZVR is the lower conversion efficiency, than it was in the case of the HERIC topology, due to the high-frequency switching pattern of the auxiliary switch S5, while in case of the HERIC topology S5 and S6 are switched with the grid frequency.

V CONCLUSION

Transformerless inverters offer a better efficiency, compared to those inverters that have a galvanic isolation. On the other hand, in case the transformer is omitted, the generated common-mode behavior of the inverter topology greatly influences the ground leakage current through the parasitic capacitance of the PV.

Bipolar PWM generates a constant common-mode voltage, but the efficiency of the converter is low, due to the two level output voltage. Using unipolar PWM modulation, the output of the converter will have three levels, but in this case the generated common-mode voltage will have high frequency components, that will lead to very high ground leakage currents.

This paper introduced a transformerless topology and gave an alternative solution for the bidirectional switch, used to generate the zero voltage state. The constant common-mode voltage of the HB-ZVR topology and its high efficiency makes it an attractive solution for transformerless PV applications.

REFERENCES

[1] "Trends in photovoltaic applications: survey report of selected IEA countries between 1992 and 2007"; Report IEA-PVPS T1-T17:2008

[2] J.M. Carrasco, L.G. Franquelo et al.; "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey"; *IEEE Transactions on Industrial Electronics*, Volume 53, Issue 4, July 2008, Page(s): 1002-1016

[3] Photon International, The Photovoltaic Magazine, Apr. 2007

[4] R. Gonzalez, J. Lopez, P. Sanchis, L. Marroyo; "Transformerless Inverter for Single-Phase Photovoltaic Systems"; *IEEE Transactions on Power Electronics*, Volume 22, Issue 2, March 2007, Page(s): 693 – 697

[5] B. Sahan, A.N. Vergara, et al.; " A Single-Stage PV Module Integrated Converter Based on a Low-Power Current-Source Inverter"; *IEEE Transactions on Industrial Electronics*, Volume 55, Issue 7, July 2008, Pages(s): 2602-2609

[6] R. Gonzalez; E. Gubia, J. Lopez, L. Marroyo; "Transformerless Single-Phase Multilevel-Based Photovoltaic Inverter"; *IEEE Transactions on Industrial Electronics*, Volume 55, Issue 7, July 2008, Page(s): 2694-2702

[7] J. Selvaraj, N.A. Rahim, "Multilevel Inverter For Grid-Connected PV System Employing Digital PI Controller"; *IEEE Transactions on Industrial Electronics*, Volume 56, Issue 1, January 2009, Page(s): 149-158

[8] E. Gubía, P. Sanchis, A. Ursúa, et al; "Ground currents in Single-phase Transformerless Photovoltaic Systems"; *Progress in Photovoltaics: Research and Applications*; 2007, Page(s): 629-650

[9] T. Kerekes, R. Teodorescu, U. Borup; "Transformerless Photovoltaic Inverters Connected to the Grid", *Applied Power Electronics Conference, APEC 2007*; 25th Feb. 2007- 1st Mar. 2007 Page(s): 1733 – 1737

[10] T. Kerekes, R. Teodorescu, C. Klumpner, M. Sumner, D. Floricau, R. Rodriguez; "Evaluation of three-phase transformerless photovoltaic inverter topologies"; *European Conference on Power Electronics and Applications*, 2nd-5th Sep. 2007, Page(s): 1-10

[11] T. Kerekes, R. Teodorescu, M. Liserre; "Common-mode voltage in case of transformerless PV inverters connected to the grid"; *International Symposium on Industrial Electronics*, ISIE 2008; 29th Jun. – 1st Jul. 2008, Page(s): 2390-2395

[12] EP 1 369 985 A2; Europeische Patentanmeldung, European Patent Office

[13] EP 1 626 494 A2; Europeische Patentanmeldung, European Patent Office

[14] D. Geibel, J. Jahn and R. Juchem; "Simulation model based control development of a multifunctional PV-inverter"; *12th European Conference on Power Electronics and Applications*; 2nd-5th Sep. 2007, Page(s): 1-10

Table 1. Efficiency at different input power with V_{dc}=350V

	500W	1000W	1500W	2000W	2500W	2800W
HB-Bip	84,37%	90,27%	92,49%	93,66%	94,28%	94,51%
HERIC	93,45%	94,71%	95,31%	95,6%	95,85%	95,94%
HB-ZVR	90,38%	92,79%	93,78%	94,39%	94,76%	94,88%

Tamás Kerekes (S'06-M'09) was born in 1978 in Cluj-Napoca, Romania. He obtained his Electrical Engineer diploma in 2002 from Technical University of Cluj, Romania, with specialization in Electric Drives and Robots. In 2005, he graduated the Master of Science program at Aalborg University, Institute of Energy Technology in the field of Power Electronics and Drives. In Sep. 2005 he began the PhD program at the Institute of Energy Technology, Aalborg University. The topic of the PhD program is: "Analysis and modeling of transformerless PV inverter systems".

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