Letters to the Editor

Reduction of Switching Losses in Active Power Filters With a New Generalized Discontinuous-PWM Strategy

Lucian Asiminoaei, Pedro Rodriguez, Frede Blaabjerg, and Mariusz Malinowski

***Abstract*—The classical discontinuous pulsewidth modulations (DPWMs) cannot be efficiently applied in active power filters (APFs) because it is difficult to predict the peak values of the inverter current. Consequently, it is difficult to calculate the optimal position of the clamped interval to minimize the switching losses in any operating point. This paper proposes a new DPWM strategy for shunt APFs. The proposed modulation strategy detects the current vector position relative to the inverter voltage reference and determines the optimum clamped duration for each phase, in terms of switching power losses. It achieves a clamped voltage pattern, with variable lengths depending on the magnitude of the inverter current. This property reduces the current stress and minimizes the inverter switching losses. The proposed modulation strategy is described, analyzed, and validated on a three-phase voltage source inverter, rated at 3 kVA, 400 V, controlled as an APF.**

***Index Terms*—Active filters, losses, power system harmonic, pulsewidth modulated inverters, reactive power, switches.**

I. Introduction

A shunt Active Power Filter (APF) is a power electronic device used for mitigating the harmonic currents from nonlinear loads [1], as is shown in Fig. 1(a). For high-power applications, the inverter cannot operate at a high switching frequency because of the considerable increase in switching losses. On the other hand, a low switching frequency is not desirable because the reduced controller bandwidth leads to improper harmonic compensation and unstable operation [2].

A potential solution that allows for an increased switching frequency is the use of discontinuous pulsewidth modulation (DPWM) [3]. Theoretically, DPWMs give an average of 33% reduction in switching losses compared to continuous PWMs, or alternatively allows an increase of the switching frequency by 33%. DPWMs have successfully been applied in unity power factor utility interface applications and induction motor drives [4]–[8]. Later researches [9]–[11] propose new types of DPWMs that adaptively track the inverter displacement power factor, deciding the optimal placement of the 60° clamped interval. However, the application is for motor drives, for sinusoidal output current.

Manuscript received August 24, 2006; revised September 17, 2007.

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Digital Object Identifier 10.1109/TIE.2007.896554

This paper proposes a discontinuous modulation strategy that detects the current vector position relative to the inverter voltage reference. The proposed algorithm calculates the duration of each clamp interval based on the "instantaneous" magnitude of the output current. Therefore, it readjusts the duration of the clamp interval each sampling time. The proposed algorithm splits and positions the clamped intervals according to the instantaneous value of the output current of an APF. This determines an adaptive clamping of the power switch that conducts the largest current at any instant, thus reducing the current stress and switching losses.

The proposed DPWM [referred to as generalized DPWM (GD-PWM)] is applied for active harmonic filtering. The GD-PWM strategy and its performance are described for a three-phase voltage source inverter rated at 3 kVA, 400 V, controlled as an APF.

II. Description of the Proposed Discontinuous Modulator

The proposed GD-PWM is based on the inverter reference voltages (V_i^*) as in the existing DPWMs, but also on the inverter reference currents (I_F^*).

The principle is illustrated in Fig. 2(a), which can easily be implemented with logical "if-then" functions. First, based on the calculated reference voltages (V_i^*), the algorithm determines the allowed clamped intervals of the pole voltage. If the selected reference voltage is allowed to be clamped, then the clamped interval of the pole voltage is set whenever the associated phase reference current is higher than the other two phases, determined internally in the APF software. Otherwise, if the selected reference voltage is not allowed to be clamped [i.e., gray shades in Fig. 2(a)], one of the other pole voltages and its associated current is used.

For comparison, Fig. 2(b) and (c) show the simulation of a typical discontinuous modulator (DPWM0) and the proposed GD-PWM for an output inverter current of 13th harmonic order. The clamped interval of 60° of the DPWM0 overlaps on two harmonic periods of the output current, while in the case of GD-PWM there are multiple clamped intervals situated around the peak value of the output current. In terms of the total area of the clamped intervals, GD-PWM gives a higher efficiency, which means an optimal reduction of the switching losses.

The algorithm of the proposed discontinuous modulation for one leg (phase-A), is presented in Fig. 3. It is performed each switching period, having the inverter reference voltages and currents as inputs. The proposed GD-PWM uses the reference voltages as delivered by the current-controller, equivalent to sinusoidal PWM modulation. The common mode voltage is then calculated (as illustrated in Fig. 3) and added to each phase reference voltages to produce the modulation signals (or the duty cycle). First, based on the reference voltages V_i^*, the algorithm determines if phase-A voltage may be clamped, otherwise, one of the other two phases is to be used. By using the reference currents, the phase current having the highest magnitude is determined. If phase-A reference current I_{Fa}^* is the largest one, then the common mode voltage is calculated such that the phase-A voltage is clamped to the positive/negative rail ([12], [13]). Otherwise, one of the other phases is clamped, but still in the condition that the clamping is allowed [14].

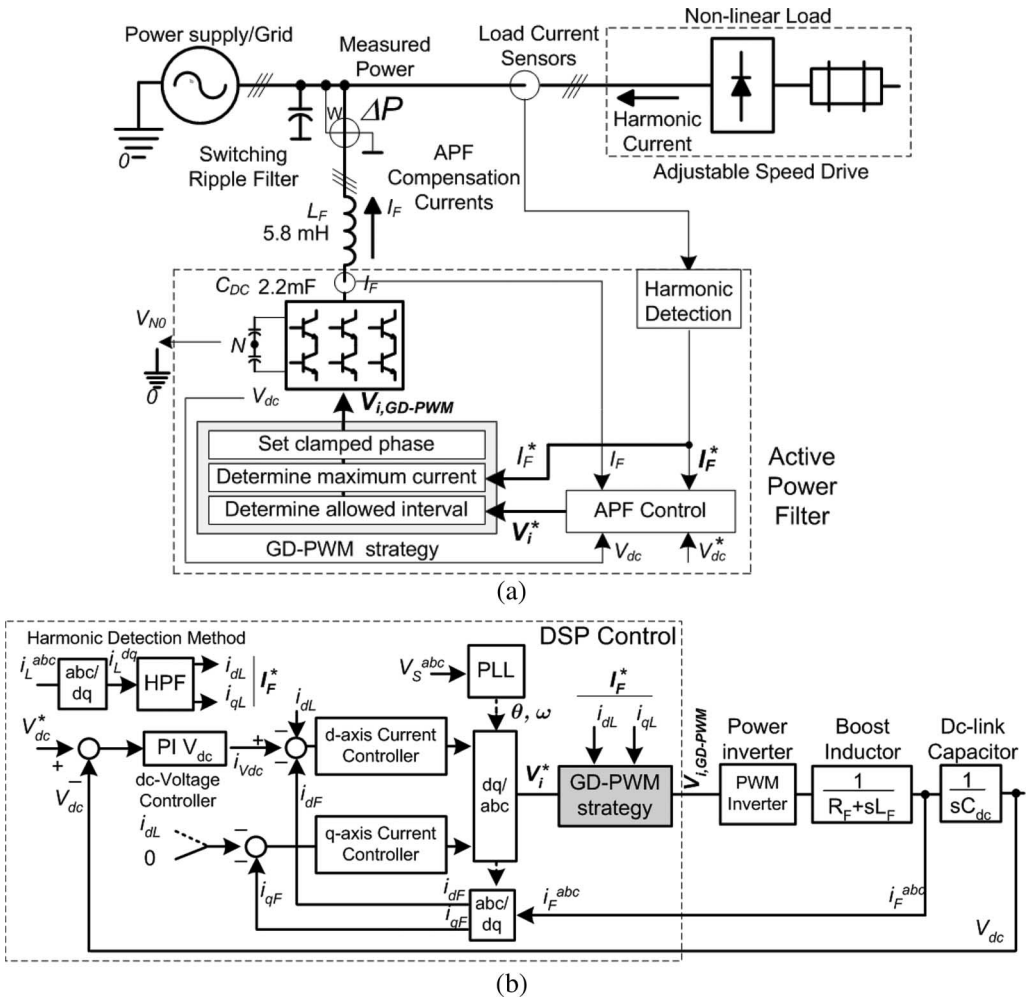

Fig. 1. Shunt APF mitigating harmonic currents from an ASD, (a) One line electrical diagram of APF connected to the system, (b) Control diagram of the APF, where the proposed GD-PWM and the other discussed modulators are implemented. The proposed modulator (GD-PWM) uses the reference voltage V_i^* and reference current I_F^* for calculation of the output voltage $V_{i,\mathrm{GD\text{-}PWM}}$.

III. Experimental Results

A test setup is realized with a 3 kVA, 400 V, VLT5006 Danfoss inverter. The line inductor has $L = 5.82$ mH inductance and a dc-link capacitor of $C_{\mathrm{dc}} = 2.2$ mF. The switching frequency can be changed from 4 to 13 kHz. A 5.5 kVA three-phase dc-smoothed diode rectifier that replicates the behavior of a typical adjustable speed drive (ASD) produces the harmonic currents.

The implementation is done in a floating-point DSP, although the PWM generation is executed by a TMS320F240, a fixed-point 16-bit DSP embedded into the dSpace board. The sampling frequency is identical to the switching frequency and the sampling is done synchronously with the PWM interrupt routine. The control algorithm is developed in the synchronous dq-reference frame. The block diagram of the proposed control [Fig. 1(b)] is a typical implementation of an APF having current controllers in the inner loop and a voltage controller in the outer loop. The switching frequency of APF was selected to be 13 kHz, which allows an easy measurement of the power losses. A detailed description of the inner current controller is given in [15].

The proposed GD-PWM is implemented by software [see Fig. 1(b)] in the existing control. The algorithm receives the reference voltages V_i^* from the current controller, and the reference harmonic currents I_F^* from the harmonic detection block as inputs [17].

Fig. 4(a) and (b) show the harmonic current compensation of APF for two types of rectifier-based ASDs having inductive or capacitive load current. The shapes of the duty cycles, which identify the output voltage $V_{i,\mathrm{GD\text{-}PWM}}$, look different in both cases. As can be seen, the duty-cycles are clamped along several intervals with different durations (depending on the output current amplitude and frequency), each time around the peak output current as illustrated by the encircled zones of the inverter current I_F.

For the inductive ASD type, the shape of the duty cycle resembles the well-known discontinuous modulator DPWM3 that has the clamped intervals in the middle, while for the capacitive ASD type, the duty cycle is closer to DPWM1 that has the clamped interval centered at the voltage peaks [9]. Both experiments prove the adaptive character of the proposed modulator depending on the position of the output current peaks.

The GD-PWM is evaluated based on the total power losses ΔP at the ac-side of the APF [see Fig. 1(a)]. The power losses in the APF are seen as disturbances in control and therefore automatically compensated by the inner and outer loop controllers. The losses were measured by connecting a power analyzer in series with the APF. The power analyzer was set to measure the power flow at the fundamental frequency. The inflow of the real power into the APF (i.e., measured power ΔP) is an estimate of the total losses, switching, and conduction of the APF.

Table I shows the power losses for both cases of inductive and capacitive ASDs, which confirms the adaptive tracking of the GD-PWM to reach minimal power losses.

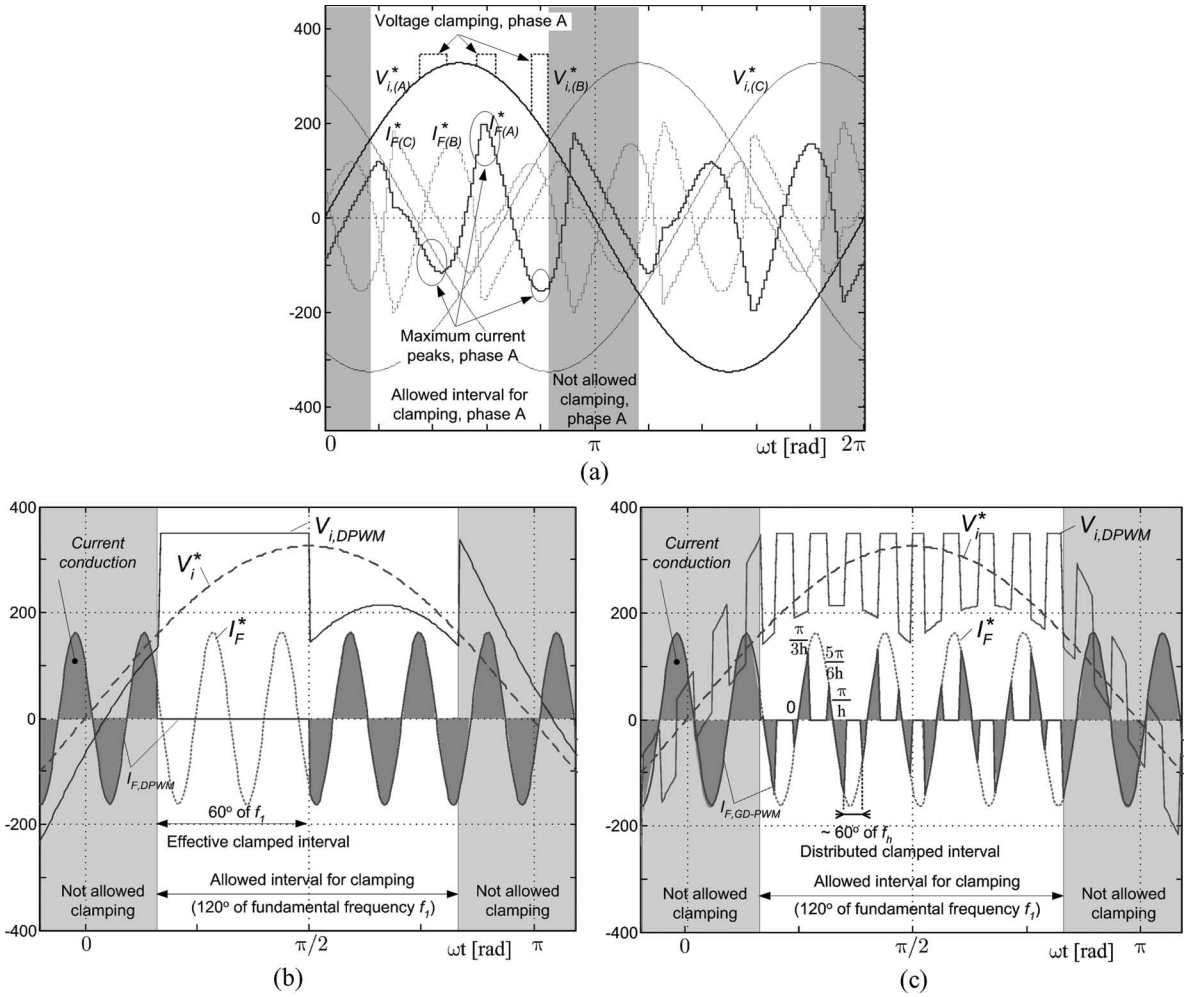

Fig. 2. Simulation of an existing and the proposed discontinuous modulator. (a) GD-PWM in active filters (both reference voltage V_i^* and reference current I_F^* are required for the calculation of the clamped intervals); (b) Clamped pole voltage for an output inverter current of 13th harmonic order using DPWM0. (c) Clamped pole voltage for an output inverter current of 13th harmonic order using the proposed GD-PWM.

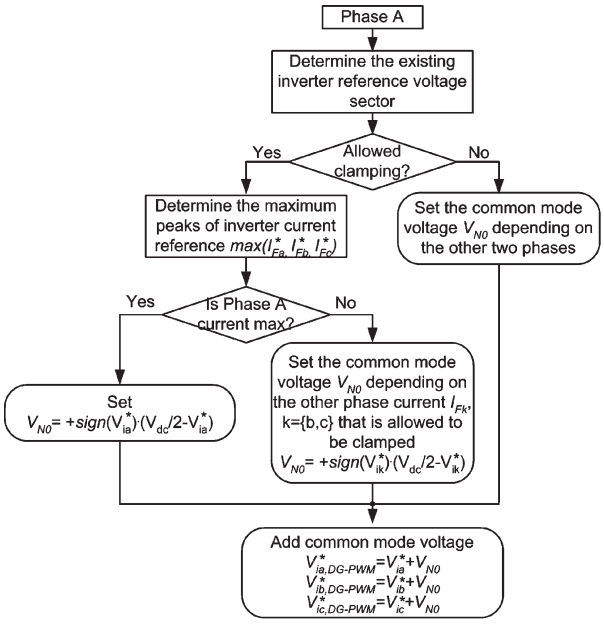

Fig. 3. Description of the logical algorithm of the proposed GD-PWM. The common mode voltages are calculated based on the allowed clamped interval and maximum current peak for each phase.

Fig. 4(c) shows the power losses ΔP for the case of the inductive ASD, which are measured at different switching frequencies. As expected, continuous modulators [i.e., sin-PWM, space vector modulation (SVM)] give higher losses, while the losses of the discontinuous modulator, including the proposed GD-PWM, depend on the position of the clamped interval. GD-PWM keeps the losses at the minimum level for the entire frequency range, which is clearly seen at a higher switching frequency.

Fig. 4(d) shows the measurement of the harmonic current distortion produced by different switching frequencies. The current distortion produced by the proposed GD-PWM is among the lowest distortion produced by the discontinuous modulators. SVM produces the lowest distortion due to its minimal phase errors [16].

IV. Conclusion

This letter describes a GD-PWM. The proposed GD-PWM is based on the detection of the current vector position relative to the inverter voltage reference, which enables the calculation of the optimum clamped duration, in terms of switching losses. It achieves spliced clamped voltage patterns, with different durations depending on the inverter peak current. This adaptively clamps the switch that conducts the largest current at any instant, which reduces the switching losses and makes the proposed modulator attractive for applications with high switching frequency.

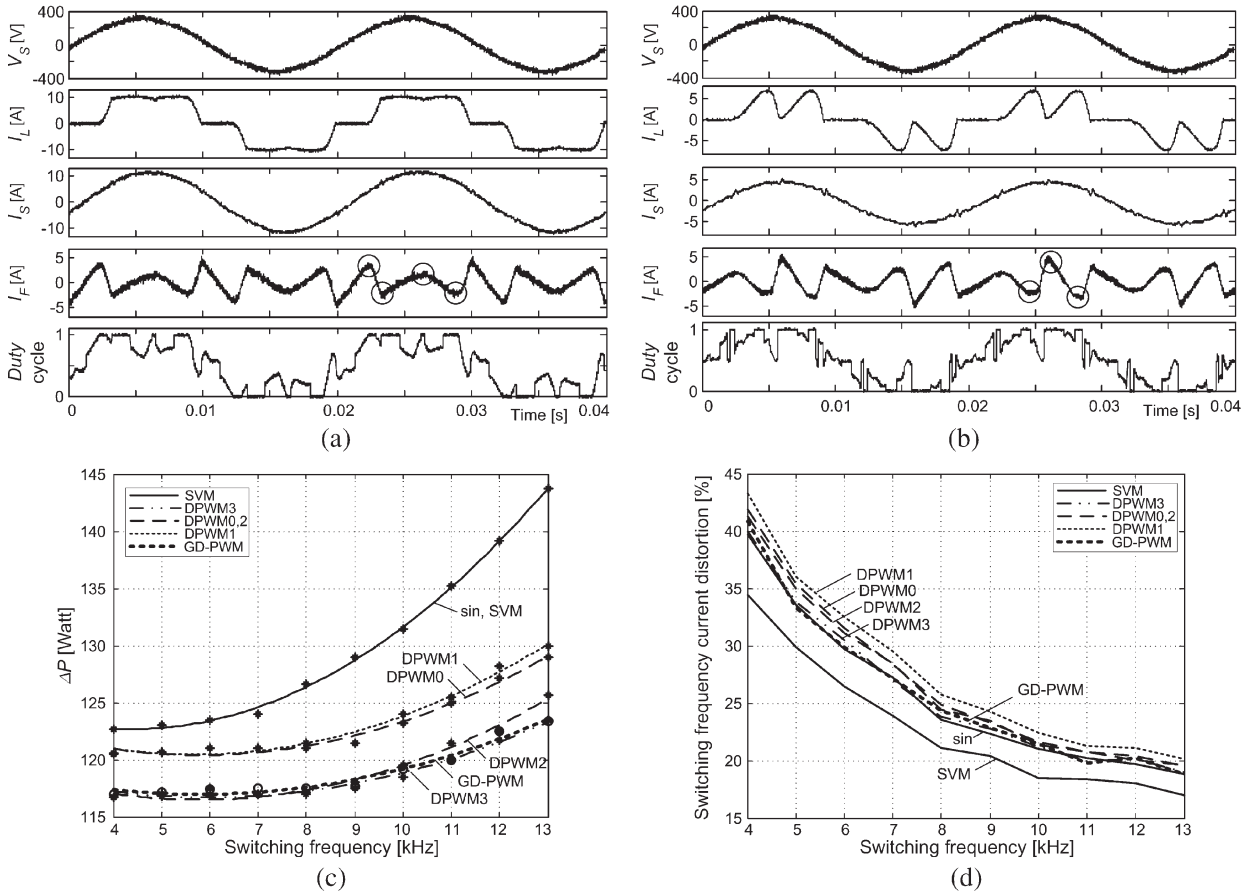

Fig. 4. Measured waveforms for APF compensating the harmonic currents from an (a) Inductive ASD, (b) Capacitive ASD (source voltage V_S, load current I_L, source current I_S, filter current I_F, and duty cycle) using the proposed GD-PWM. (c) Measured power losses ΔP using the presented modulators at different switching frequencies, for harmonic current compensation as shown in Fig. 4(a) (inductive ASD). (d) Measured switching frequency current distortion of the APF for sinusoidal output reactive current of 2.5 A_{rms}, using the presented modulators at different switching frequencies.

TABLE I
COMPARISON OF THE MEASURED POWER LOSSES AT 13 kHz SWITCHING FREQUENCY, GIVEN BY DIFFERENT TYPES OF MODULATORS

Modulator	ΔP [W] (inductive ASD)	ΔP [W] (capacitive ASD)
Space vector modulation (SVM)	144	148
Discontinuous PWM with placement of zero vector at 0°: DPWM0	130	132
Discontinuous PWM with placement of zero vector at 30°: DPWM1	131	126
Discontinuous PWM with placement of zero vector at 60°: DPWM2	125	125
Discontinuous PWM with placement of zero vector at 90°: DPWM3	123	130
Proposed GD-PWM	123	125

The experiments done on a three-phase power inverter rated at 3 kVA, 400 V show that the proposed GD-PWM is a type of discontinuous modulator that adapts according to the amplitude and shape of the output current. The measured losses and harmonic distortion of the GD-PWM reach minimum levels among discontinuous modulators, regardless of its application.

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Cost-Effective Boost Converter With Reverse-Recovery Reduction and Power Factor Correction

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***Abstract*—A boost converter with high performance and low cost is proposed for power factor correction. The proposed boost converter reduces the reverse-recovery loss of the diode by adding a simple inductor-diode branch paralleled with the output diode. Detailed analysis and experimental results obtained on a 300-W prototype are discussed.**

***Index Terms*—Boost converter, power factor correction (PFC).**

I. Introduction

Recently, low harmonic equipment in industrial electronic applications has been recommended by a European regulation (EN 61000-3-2) and IEEE standard (IEEE 519). In an effort to meet these requirements, a continuous-conduction-mode (CCM) boost converter has been widely used for power factor correction (PFC). The converter is praised for its high power capability and high power factor. To achieve high power density and faster transient response, the converter should operate at a high switching frequency. However, as the switching frequency increases, the output diode operated in high voltage provides significant reverse-recovery loss in a hard-switching boost converter. The reverse-recovery problem of the output diode affects the switching devices in the form of additional turn-on loss. The reverse-recovery loss of the diode is the most significant due to its large current at the minimum input voltage. Other adverse effects of the reverse-recovery problem include electromagnetic interference and additional thermal management.

Manuscript received January 20, 2005; revised September 6, 2007.

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Digital Object Identifier 10.1109/TIE.2007.896526

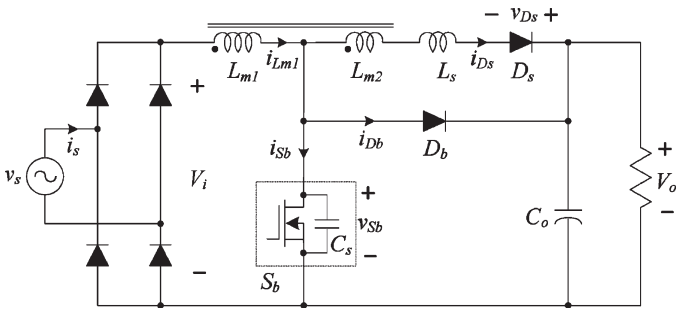

Fig. 1. Proposed boost converter.

To overcome these problems, various passive snubber approaches have been proposed and silicon carbide (SiC) Schottky diodes were developed [1]–[5]. However, the snubber in [1] has the limitation of the duty cycle range for PFC. A method with coupled inductors is presented in [2] for a wider operation range of the snubber. Although the coupled inductors improve the snubber operation, the snubber still has the problem of an increased voltage or current stress. Furthermore, the circulating current due to the resonant circuit produces additional conduction loss [2], [3]. Meanwhile, the SiC Schottky diode makes it possible to improve the reverse-recovery problem of the fast recovery diode in a conventional boost converter. However, its major drawback is the high cost.

In this letter, a cost-effective implementation for a CCM boost converter is proposed. Adding one coupled inductor to an inductor-diode branch, the reverse-recovery loss of the output diode is reduced without any significantly increased component stress. Experiment results based on a 300-W prototype are obtained to show the performance of the proposed boost converter.

II. Analysis of Proposed Boost Converter

The proposed converter shown in Fig. 1 is basically the simple boost topology having an inductor L_{m1}, a boost switch S_{b} with its internal capacitance C_{s}, an output boost diode D_{b}, and an output capacitor C_{o}. It also has an additional branch consisting of a coupled inductor L_{m2}, an inductor L_{s}, and a diode D_{s} parallel with the output diode D_{b}. The inductor L_{m1} and inductor L_{m2} are magnetically coupled with a turns ratio of $1 : N (N \ll 1)$ and negligible leakage inductances. During one switching period $T_{\mathrm{s}} (= 1/f_{\mathrm{s}})$, the output voltage V_{o} and the rectified voltage V_{i} from the line voltage ν_{s} are considered to be constant. The inductor L_{m1} is much greater than the inductor L_{s}.

The converter given in Fig. 1 has six distinct operating modes with duty ratio D during one switching period T_{s}. The duty ratio of the CCM boost converter determines the following voltage relation:

$$\frac{V_{\mathrm{o}}}{V_{\mathrm{i}}} = \frac{1}{1-D} \tag{1}$$