A Virtual-Vector Pulsewidth Modulation for the Four-Level Diode-Clamped DC–AC Converter

Sergio Busquets-Monge, *Member, IEEE*, Josep Bordonau, *Member, IEEE*, and Joan Rocabert

***Abstract*—Several pulsewidth modulation (PWM) strategies have been proposed for the three-level three-phase diode-clamped dc–ac converter. Among them, the nearest-three virtual-space-vector PWM guarantees the dc-link capacitor voltage balance under any operating condition, provided that the addition of the three phase currents equals zero. This paper extends this modulation concept to the four level converter. The new virtual vectors are presented and a simple modulation solution is defined. Conventional nearest-three space vector PWM cannot comprehensively achieve balanced and stable dc-link voltages. The proposed modulation solution enables the practical use of the four-level converter since it guarantees the dc-link capacitor voltage balance for any operating condition and load, provided that the addition of the three phase currents equals zero. Simulation and experimental results prove the goodness of the presented approach.**

***Index Terms*—Capacitor voltage balance, diode-clamped, multilevel, pulsewidth modulation (PWM), virtual vector.**

I. Introduction

MULTILEVEL converter topologies [1], [2], have received special attention during the last two decades due to their significant advantages compared to the conventional two level case. These topologies allow reducing the voltage across the semiconductors without the problems associated to the series interconnection of devices, reduce the harmonic distortion of the output voltage and improve the efficiency of the converter. However, a larger number of semiconductors is needed and the modulation strategy to control them becomes more complex.

Multilevel converters are typically considered for high power applications, because they allow operating at higher dc-link voltage levels with the current available semiconductor technology. But they can also be interesting for medium or even low power/voltage applications, since they allow operating with lower voltage-rated devices, with potentially better performance/economical features [3], [4].

There are three basic multilevel converter topologies: diode-clamped, flying capacitor, and cascaded H-bridge with separate dc sources. Among these topologies, diode-clamped converters are especially interesting because of their simplicity: the multiple voltage levels are generated passively through a set of series-connected capacitors. However, these topologies present the challenging problem of balancing the dc-link capacitor voltages to guarantee equal voltage sharing among the devices and good performance features.

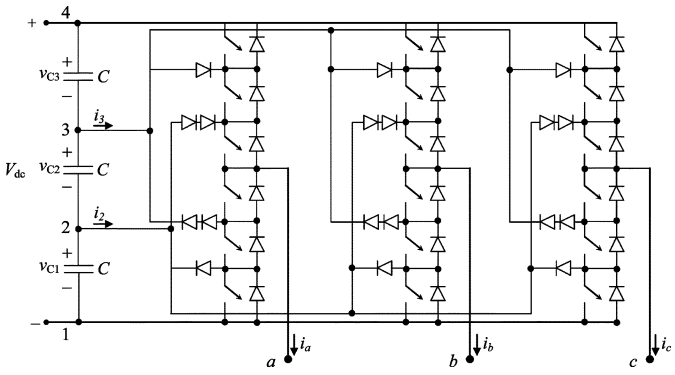

Fig. 1. Four-level three-phase diode-clamped dc–ac converter.

Among diode-clamped topologies, the three-level three-phase diode-clamped dc–ac converter [5] is the most popular. Several modulation strategies have been proposed for this converter. Conventional pulsewidth modulations (PWMs) are based on the selection of the nearest-three space vectors (NTV). However, as demonstrated in [6], these PWMs are not capable of balancing the voltage of the dc-link capacitors under certain operating conditions. On the other hand, the nearest-three virtual-space-vector (NTV^2) PWM [7] is capable of controlling the dc-link capacitor voltage balance for any load (linear or non-linear, balanced or unbalanced) and modulation index, provided that the addition of the output three-phase currents equals zero. Reference [8] shows how to interface this modulation with conventional closed-loop control schemes, and develops a specific control to mitigate possible dc-link voltage balance perturbations.

Several studies have focused on diode-clamped topologies with higher levels, in particular the four-level three-phase diode-clamped dc–ac converter in Fig. 1 [9]–[13]. They conclude that the use of NTV PWM with the four-level converter cannot achieve dc-link capacitor voltage balance under a substantial portion of the converter operating conditions. Eventually, these operating conditions lead to instabilities in the balance, causing the voltage of the middle capacitor to collapse; i.e., the capacitor voltages do not balance over the fundamental period. The limits for balanced and stable operation are specified in [13].

To overcome these limitations of diode-clamped topologies with more than three levels, some authors propose the addition

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The authors are with the Department of Electronic Engineering, Technical University of Catalonia, Barcelona 08028, Spain (e-mail: sergio.busquets@upc.edu).

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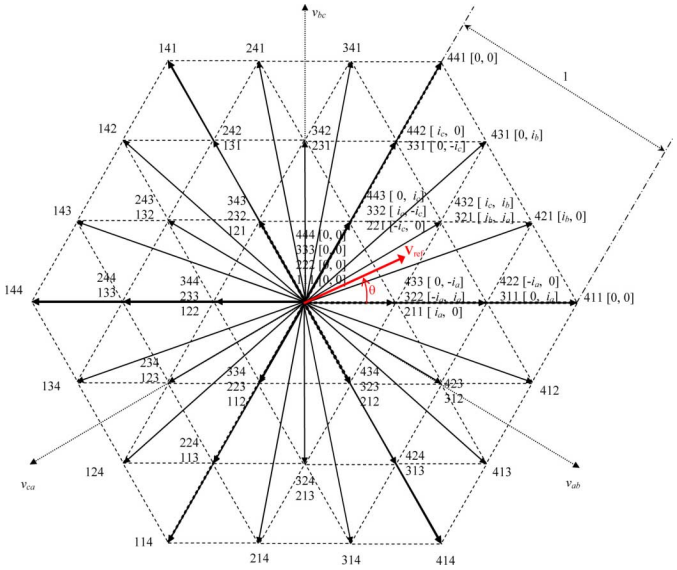

Fig. 2. Normalized space vector diagram for the four-level three-phase diode-clamped dc–ac converter.

of circuitry specifically designed to guarantee the balance [14], [15]. Others introduce a fourth leg [16]. And finally, others use a back-to-back connection of multilevel converters to extend the operating range through which the balance can be guaranteed [17]–[19]. The majority of authors, though, have discarded the use of diode-clamped converters with more than three levels in favor of other topologies: flying capacitor, cascaded H-bridge with separate dc sources, and hybrid converter topologies.

In this paper, the virtual-vector concept presented in [7] is extended to the four-level diode-clamped converter. A virtual-vector-based PWM is then derived. The resulting PWM scheme guarantees the dc-link voltage balance for any modulation index and load, provided that the addition of the three phase currents equals zero. Hence, this modulation enables the practical use of the four-level converter with passive front ends and only requires small dc-link capacitors.

The paper is organized as follows. In Section II, the proposed modulation scheme is defined. In Sections III and IV, the performance of this modulation is analyzed and compared to a reference NTV modulation through both simulations and experiments, and Section V outlines the conclusions.

II. Minimum-Perimeter Triangles Virtual-Space-Vector PWM

A. Virtual-Space-Vector Definition

Fig. 2 shows the space vector diagram (SVD) for the four-level diode-clamped dc–ac converter. The converter has 64 switching states corresponding to all the combinations of connections of each phase to the dc-link points 1–4; e.g., 432, corresponding to the connection of phase a to point 4, phase b to 3, and phase c to 2. These switching states define 37 space vectors.

In the conventional NTV PWM, the reference vector $(V_{\text{ref}}) = m{\cdot}e^{i\,\theta} = (m{\cdot}\cos(\theta), m{\cdot}\sin(\theta))_{\alpha,\beta} = ((V_{\text{ref}\alpha}, V_{\text{ref}\beta})_{\alpha,\beta}), (m \in [0,1]$ for linear modulation) is synthesized in each switching cycle (with period $T_s = 1/f_s$; f_s is the carrier/sampling frequency) by a sequence of the nearest three vectors. Whenever a vector can be generated by more than one switching state, an additional selection of one switching state or a combination of several has to be made.

Due to the six-fold symmetry of the SVD, only one sextant needs to be analyzed to define a modulation strategy. In the first sextant of the SVD of Fig. 2, the midpoint (MP) currents i_2 and i_3 corresponding to each switching state are specified in brackets: $[i_2, i_3]$. Analogous to the three-level case, the average i_2 and average i_3 in every switching cycle must be zero to guarantee the dc-link capacitor voltage balance. In the NTV PWM, whenever redundant switching states are available for a given space vector, the appropriate combination of these switching states must be selected to guarantee that the average MP currents equal zero in every switching cycle. However, this is not possible for high modulation indexes, especially when the load angle is small ($m_{\max} = 0.55$ for a zero load angle [13]).

To achieve full control of the dc-link capacitor voltage balance, a set of new virtual vectors (VVs) is defined as a linear combination of the vectors corresponding to certain switching states. The new virtual vectors, shown in Fig. 3 for the first sextant of the SVD, are defined in

$$\mathbf{V}_1 = \frac{1}{2}(333) + \frac{1}{2}(222) = (0,0)_{\alpha,\beta}$$

$$\mathbf{V}_2 = \frac{1}{3}(433) + \frac{1}{3}(322) + \frac{1}{3}(211) = \left(\frac{2}{3\sqrt{3}}, 0\right)_{\alpha,\beta}$$

$$\mathbf{V}_3 = \frac{1}{3}(443) + \frac{1}{3}(332) + \frac{1}{3}(221) = \left(\frac{1}{3\sqrt{3}}, \frac{1}{3}\right)_{\alpha,\beta}$$

$$\mathbf{V}_4 = \frac{1}{4}(443) + \frac{1}{4}(432) + \frac{1}{4}(321) + \frac{1}{4}(211) = \left(\frac{\sqrt{3}}{4}, \frac{1}{4}\right)_{\alpha,\beta}$$

$$\mathbf{V}_{5,1} = \frac{1}{2}(422) + \frac{1}{2}(211) = \left(\frac{1}{\sqrt{3}}, 0\right)_{\alpha,\beta}$$

$$\mathbf{V}_{5,2} = \frac{1}{2}(433) + \frac{1}{2}(311) = \left(\frac{1}{\sqrt{3}}, 0\right)_{\alpha,\beta}$$

$$\mathbf{V}_{6,1} = \frac{1}{2}(442) + \frac{1}{2}(221) = \left(\frac{1}{2\sqrt{3}}, \frac{1}{2}\right)_{\alpha,\beta}$$

$$\mathbf{V}_{6,2} = \frac{1}{2}(443) + \frac{1}{2}(331) = \left(\frac{1}{2\sqrt{3}}, \frac{1}{2}\right)_{\alpha,\beta}$$

$$\mathbf{V}_7 = \frac{1}{5}(443) + \frac{1}{5}(432) + \frac{1}{5}(421) + \frac{1}{5}(311) + \frac{1}{5}(211) = \left(\frac{1}{\sqrt{3}}, \frac{1}{5}\right)_{\alpha,\beta}$$

$$\mathbf{V}_8 = \frac{1}{5}(443) + \frac{1}{5}(442) + \frac{1}{5}(431) + \frac{1}{5}(321) + \frac{1}{5}(211) = \left(\frac{4}{5\sqrt{3}}, \frac{2}{5}\right)_{\alpha,\beta}$$

$$\mathbf{V}_{9,1} = \frac{1}{3}(442) + \frac{1}{3}(421) + \frac{1}{3}(211) = \left(\frac{1}{\sqrt{3}}, \frac{1}{3}\right)_{\alpha,\beta}$$

$$\mathbf{V}_{9,2} = \frac{1}{3}(443) + \frac{1}{3}(431) + \frac{1}{3}(311) = \left(\frac{1}{\sqrt{3}}, \frac{1}{3}\right)_{\alpha,\beta}$$

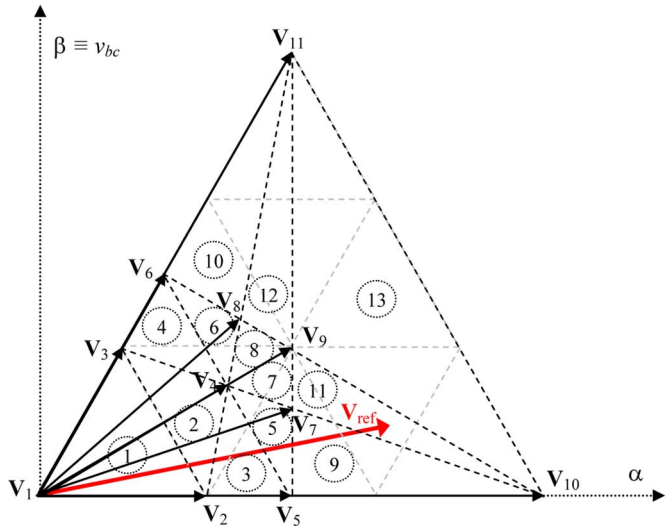

Fig. 3. Virtual space vectors for the first sextant of the SVD.

$$\mathbf{V}_{10} = (411) = \left(\frac{2}{\sqrt{3}}, 0\right)_{\alpha,\beta}$$
$$\mathbf{V}_{11} = (441) = \left(\frac{1}{\sqrt{3}}, 1\right)_{\alpha,\beta}. \quad (1)$$

These vectors have associated average MP currents in every switching cycle equal to zero, due to analogous reasons as those discussed for the three-level converter [7].

Note that virtual vectors $\mathbf{V}_5$, $\mathbf{V}_6$ and $\mathbf{V}_9$ present redundancy. There are two possible elementary combinations of switching states to define each VV ($\mathbf{V}_{5,1}$ and $\mathbf{V}_{5,2}$ for $\mathbf{V}_5$; $\mathbf{V}_{6,1}$ and $\mathbf{V}_{6,2}$ for $\mathbf{V}_6$; $\mathbf{V}_{9,1}$ and $\mathbf{V}_{9,2}$ for $\mathbf{V}_9$). In fact, any combination of both elementary options can be used to implement virtual vectors $\mathbf{V}_5$, $\mathbf{V}_6$ and $\mathbf{V}_9$, see (2), shown at the bottom of the page, where x_5, x_6, $x_9 \in [0, 1]$.

A particularly interesting combination is obtained when $x = 0.5$, since it represents an equitable combination of all switching states involved.

B. Virtual Space Vector Selection

In each switching cycle, a set of VVs needs to be selected to synthesize the reference vector. First, the first sextant of the SVD will be divided into a set of disjoint triangular regions. Among all possible triangles defined joining the tips of compatible VVs (VVs with switching states that can be arranged to follow the sequence defined in Section II-C), the one having the minimum perimeter is initially selected. Next, among all other possible disjoint triangles, the one having the minimum perimeter is also chosen. This process is repeated until the selected triangles completely cover the first sextant. An alternative simple procedure to obtain this division of the first sextant into disjoint minimum-perimeter triangles is:

1) draw lines connecting each VV tip with the tip of every other compatible VV available;
2) if two lines are crossing, discard the longer one.

Thirteen triangles result, as shown in the diagram of Fig. 3. Since the selection of the triangular regions dividing the first sextant is a key step in the definition of the modulation strategy proposed in this work, it is designated as the minimum-perimeter triangles virtual-space-vector (MTV^2) PWM.[1]

The synthesis of the reference vector in each switching cycle is performed using the three VVs defining the vertices of the triangular region where the tip of V_{ref} is located. Table I specifies these selected VVs for each region.

TABLE I
SELECTION OF VVS FOR EACH TRIANGULAR REGION

Region	Selected VV
1	$\mathbf{V}_1$, $\mathbf{V}_2$, $\mathbf{V}_3$
2	$\mathbf{V}_2$, $\mathbf{V}_3$, $\mathbf{V}_4$
3	$\mathbf{V}_2$, $\mathbf{V}_4$, $\mathbf{V}_5$
4	$\mathbf{V}_3$, $\mathbf{V}_4$, $\mathbf{V}_6$
5	$\mathbf{V}_4$, $\mathbf{V}_5$, $\mathbf{V}_7$
6	$\mathbf{V}_4$, $\mathbf{V}_6$, $\mathbf{V}_8$
7	$\mathbf{V}_4$, $\mathbf{V}_7$, $\mathbf{V}_9$
8	$\mathbf{V}_4$, $\mathbf{V}_8$, $\mathbf{V}_9$
9	$\mathbf{V}_5$, $\mathbf{V}_7$, $\mathbf{V}_{10}$
10	$\mathbf{V}_6$, $\mathbf{V}_8$, $\mathbf{V}_{11}$
11	$\mathbf{V}_7$, $\mathbf{V}_9$, $\mathbf{V}_{10}$
12	$\mathbf{V}_8$, $\mathbf{V}_9$, $\mathbf{V}_{11}$
13	$\mathbf{V}_9$, $\mathbf{V}_{10}$, $\mathbf{V}_{11}$

The duty ratio of each selected vector in each switching cycle is calculated as

$$\begin{aligned} \mathbf{V}_{\text{ref}} &= d_{VV1} \cdot \mathbf{VV}_1 + d_{VV2} \cdot \mathbf{VV}_2 + d_{VV3} \cdot \mathbf{VV}_3 \\ 0 &\le d_{VVj} \le 1, \quad j = 1, 2, 3 \\ d_{VV1} &+ d_{VV2} + d_{VV3} \\ &= 1 \end{aligned} \quad (3)$$

where $\mathbf{VV}_j$ corresponds to the jth selected virtual space vector.

[1]The process outlined here can also be applied to define the five triangular regions dividing the first sextant of the three-level converter SVD in [7]. Therefore, the modulation proposed in [7] belongs to the family of MTV^2 PWMs. In fact, in some areas of region 1 [7] the true nearest-three VVs are not employed to approximate the reference vector. Hence, the chosen designation (NTV^2 PWM) is not entirely appropriate for this region.

$$\begin{aligned} \mathbf{V}_5(x_5) &= x_5 \cdot \mathbf{V}_{5,1} + (1 - x_5) \cdot \mathbf{V}_{5,2} = \frac{x_5}{2}(422) + \frac{x_5}{2}(211) + \frac{1 - x_5}{2}(433) + \frac{1 - x_5}{2}(311) \\ \mathbf{V}_6(x_6) &= x_6 \cdot \mathbf{V}_{6,1} + (1 - x_6) \cdot \mathbf{V}_{6,2} = \frac{x_6}{2}(442) + \frac{x_6}{2}(221) + \frac{1 - x_6}{2}(443) + \frac{1 - x_6}{2}(331) \\ \mathbf{V}_9(x_9) &= x_9 \cdot \mathbf{V}_{9,1} + (1 - x_9) \cdot \mathbf{V}_{9,2} = \frac{x_9}{3}(442) + \frac{x_9}{3}(421) + \frac{x_9}{3}(211) + \frac{1 - x_9}{3}(443) + \frac{1 - x_9}{3}(431) + \frac{1 - x_9}{3}(311) \end{aligned} \quad (2)$$

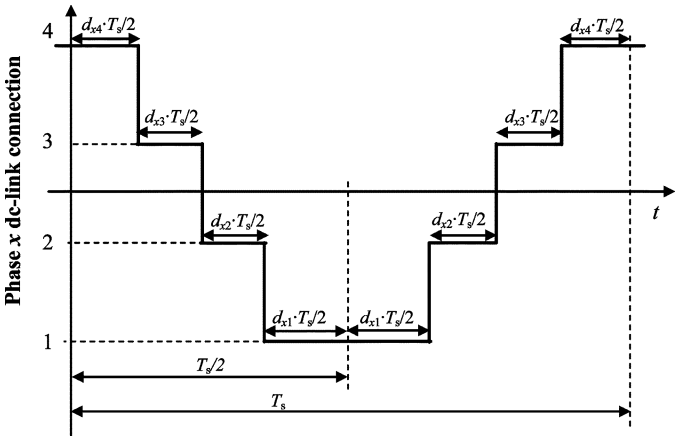

Fig. 4. Selected sequence of connection of phase x (a, b or c) to each of the dc-link points (1, 2, 3, and 4).

Then, the corresponding duty ratio of the different switching states can be calculated. For the first sextant

$$
\begin{aligned}
&d_{222} = d_{333} = \frac{1}{2}d_{\mathbf{V}1}, \quad d_{433} = \frac{1}{3}d_{\mathbf{V}2} + \frac{1-x_5}{2}d_{\mathbf{V}5}\\
&d_{322} = \frac{1}{3}d_{\mathbf{V}2}, \quad d_{332} = \frac{1}{3}d_{\mathbf{V}3}, \quad d_{432} = \frac{1}{4}d_{\mathbf{V}4} + \frac{1}{5}d_{\mathbf{V}7}\\
&d_{211} = \frac{1}{3}d_{\mathbf{V}2} + \frac{1}{4}d_{\mathbf{V}4} + \frac{x_5}{2}d_{\mathbf{V}5} + \frac{1}{5}d_{\mathbf{V}7} + \frac{1}{5}d_{\mathbf{V}8} + \frac{x_9}{3}d_{\mathbf{V}9}\\
&d_{443} = \frac{1}{3}d_{\mathbf{V}3} + \frac{1}{4}d_{\mathbf{V}4} + \frac{1-x_6}{2}d_{\mathbf{V}6}\\
&\qquad + \frac{1}{5}d_{\mathbf{V}7} + \frac{1}{5}d_{\mathbf{V}8} + \frac{1-x_9}{3}d_{\mathbf{V}9}\\
&d_{221} = \frac{1}{3}d_{\mathbf{V}3} + \frac{x_6}{2}d_{\mathbf{V}6},\\
&d_{321} = \frac{1}{4}d_{\mathbf{V}4} + \frac{1}{5}d_{\mathbf{V}8}, \quad d_{422} = \frac{x_5}{2}d_{\mathbf{V}5}\\
&d_{311} = \frac{1-x_5}{2}d_{\mathbf{V}5} + \frac{1}{5}d_{\mathbf{V}7} + \frac{1-x_9}{3}d_{\mathbf{V}9}\\
&d_{442} = \frac{x_6}{2}d_{\mathbf{V}6} + \frac{1}{5}d_{\mathbf{V}8} + \frac{x_9}{3}d_{\mathbf{V}9}\\
&d_{331} = \frac{1-x_6}{2}d_{\mathbf{V}6}, \quad d_{431} = \frac{1}{5}d_{\mathbf{V}8} + \frac{x_9}{3}d_{\mathbf{V}9}\\
&d_{421} = \frac{1}{5}d_{\mathbf{V}7} + \frac{x_9}{3}d_{\mathbf{V}9}, \quad d_{411} = d_{\mathbf{V}10}, \quad d_{441} = d_{\mathbf{V}11}. \quad (4)
\end{aligned}
$$

C. Switching States Sequence

Finally, the sequence over time within a switching cycle of the application of the different switching states has to be decided. The chosen switching states' order is such that the sequence of connection of each phase to the dc-link points is the symmetrical 4-3-2-1-2-3-4, as shown in Fig. 4. This can be achieved by simply ordering the switching-states three-digit number in descending-ascending order.

Therefore, a practical implementation of the proposed modulation strategy only requires the computation of duty ratios d_{a1}, d_{b1}, d_{c1}, d_{a2}, d_{b2}, d_{c2}, d_{a3}, d_{b3}, d_{c3}, d_{a4}, d_{b4}, d_{c4} (where d_{xy} is the duty ratio of the phase x connection to the dc-link point y), as the addition of the appropriate switching state duty ratios calculated in Section II-B. For example, in the first sextant, to obtain d_{a2}

$$d_{a2} = d_{222} + d_{221} + d_{211}. \quad (5)$$

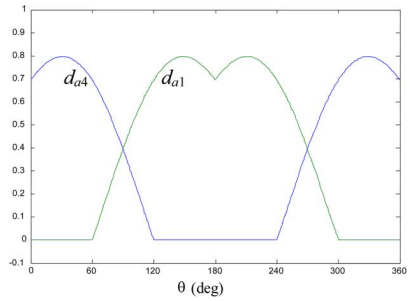

Fig. 5. d_{a1} and d_{a4} as a function of $\theta (m = 0.8)$.

D. Phase Duty-Ratio Expressions

Fig. 5 shows the simulated duty ratios d_{a1} and d_{a4}, for any MTV^2 PWM, $m = 0.8$ and a line period. The simple pattern observed for d_{a4} can be mathematically expressed as

$$
\begin{aligned}
0 \le \theta < \frac{2\pi}{3} &: d_{a4} = m \cdot \cos\left(\theta - \frac{\pi}{6}\right)\\
\frac{2\pi}{3} \le \theta < \frac{4\pi}{3} &: d_{a4} = 0\\
\frac{4\pi}{3} \le \theta < 2\pi &: d_{a4} = m \cdot \cos\left(\theta + \frac{\pi}{6}\right). \quad (6)
\end{aligned}
$$

The expression for duty ratio d_{a1} is the same as (6) but phase-shifted 180°. The expressions for the b and c phase duty ratios are the same as for phase a, but phase shifted 120° and 240°, respectively. Note that these expressions are the same as for d_{an}, d_{bn}, d_{cn}, d_{ap}, d_{bp}, and d_{cp} in the three-level converter [7].

For convenience in the interfacing of the modulation strategy to a conventional control scheme, (6) and the like for the remaining phase duty-ratios can also be expressed in terms of $V_{\mathrm{ref}\alpha}$ and $V_{\mathrm{ref}\beta}$ as in

$$
\begin{aligned}
0 \le \theta < \frac{2\pi}{3} &: d_{a4} = \left(\frac{\sqrt{3}}{2}\right) \cdot V_{\mathrm{ref}\alpha} + \left(\frac{1}{2}\right) \cdot V_{\mathrm{ref}\beta}\\
\frac{2\pi}{3} \le \theta < \frac{4\pi}{3} &: d_{a4} = 0\\
\frac{4\pi}{3} \le \theta < 2\pi &: d_{a4} = \left(\frac{\sqrt{3}}{2}\right) \cdot V_{\mathrm{ref}\alpha} - \left(\frac{1}{2}\right) \cdot V_{\mathrm{ref}\beta}. \quad (7)
\end{aligned}
$$

The expressions for d_{a2}, d_{b2}, d_{c2}, d_{a3}, d_{b3}, and d_{c3} depend upon the selection of x_5, x_6, and x_9; i.e., the combination of redundant VVs employed to implement V_5, V_6, and V_9. A choice of $x_5, x_6, x_9 = 0.5$ seems to be good a priori, since all possible redundant VVs are then equally employed in approximating the reference vector.

The resulting expressions for d_{a2}, d_{a3}, d_{b2}, d_{b3}, d_{c2}, and d_{c3} are very simple:

$$
\begin{aligned}
d_{a2} &= d_{a3} = d_{b2} = d_{b3} = d_{c2} = d_{c3}\\
&= \frac{1 - d_{a1} - d_{a4}}{2} = \frac{1 - d_{b1} - d_{b4}}{2} = \frac{1 - d_{c1} - d_{c4}}{2}. \quad (8)
\end{aligned}
$$

TABLE II
COMPARISON OF NTV AND MTV^2 PWM UNDER DIFFERENT SCENARIOS

Scenario	Advantages NTV PWM	Advantages MTV^2 PWM
1. Multilevel converter connected to a single dc bus and without balancing closed-loop control [22]	• None (dc-link capacitor voltages collapse)	• Balanced dc-link capacitor voltages operation is achieved under ideal or quasi-ideal operating conditions
2. Multilevel converter connected to a single dc bus and with a balancing closed-loop control [22]	• None	• More effective balancing control (faster dynamical response) • Lower computation time (around 5% of the time required with NTV PWM)
3. Multilevel converter with regulated dc voltage sources replacing the dc-link capacitors	• Lower THD • Lower switching losses in the multilevel converter	• Lower computation time
4. Multilevel converter with unregulated dc voltage sources replacing the dc-link capacitors.	• Lower THD • Lower switching losses in the multilevel converter	• No low frequency distortion appears in the output ac voltages if the voltage sources are different in value • Lower computation time

The expressions in (7) and (8) allow obtaining directly $d_{a1}, d_{b1}, d_{c1}, \ldots, d_{a4}, d_{b4}$, and d_{c4} as a function of the reference vector coordinates, without the need of identifying the triangle in which the reference vector is located and then performing calculations (3)–(5). This significantly simplifies the computations. The Appendix contains a simple algorithm to implement this PWM in the full line cycle. Notice that no trigonometric functions need to be evaluated.

The modulation solution defined by (7) and (8) presents seven pairs of switching transitions (one switch turns off and another turns on) per half switching cycle in all 13 regions of the SVD.

A different choice of x_5, x_7, and x_9 (values of 0 or 1 are especially interesting to test) leads to different modulation solutions with potentially lower ac-side harmonic distortion and lower number of switching transitions (see examples in [20]) but they will not be considered here for the sake of simplicity (they lead to more complex phase duty-ratio waveform patterns).

III. SIMULATION RESULTS

The performance of the proposed modulation has been analyzed through simulation in Matlab-Simulink and compared to a particular NTV PWM. In this modulation used as a reference for comparison, the duty ratio assigned to each space vector is equally shared in every switching cycle by all associated switching states. Compared to other possible NTV PWM solutions, this particular NTV PWM presents a minimum output voltage distortion [21], but uses a greater number of switching transitions per switching cycle at low modulation indices.

Table II presents a summary of the advantages of the reference NTV PWM and proposed MTV^2 PWM under four different scenarios. For the sake of simplicity, an inverter operation mode of the multilevel converter is assumed (average power flows from the dc side to the ac side).

In scenario 1, the multilevel converter in Fig. 1 is connected to a single dc bus through terminals 1 and 4. The dc bus can be generated, for instance, from the mains or other ac sources employing a simple diode rectifier. In this case, the use of any open-loop NTV PWM leads to the collapse of the middle capacitor voltage. Therefore, in this scenario, NTV PWMs have no meaningful application in practice, since they would produce an excessive voltage stress in some of the devices and severe low-frequency output voltage distortion. The use of an open-loop MTV^2 PWM, instead, produces balanced dc-link capacitor voltages under ideal or quasi-ideal operating conditions (addition of phase currents equal to zero, similar switching behavior of the different devices, etc.) with small dc-link capacitors. Fig. 6 presents the results of the comparison at $m = 0.75$ for the phase a duty ratios and the dc-link capacitor voltages. As expected, the proposed modulation guarantees the dc-link balance while the NTV PWM not only can not guarantee the balance but also leads to the collapse of v_{C2}.

In scenario 2, the addition of a balancing closed-loop control [22] is considered. Since the NTV PWM has no natural balancing and stability properties, the closed-loop control will necessarily have to modify the preexisting NTV PWM phase duty ratios into the phase duty ratios of a given virtual-vector-based PWM in order to guarantee the capacitor voltage balance (switching losses and THD will then be similar to the MTV^2 PWM, if not worse). Although this is plausible, it can be recognized that it would require a significant control effort, and the dynamical response of the control under perturbations in the balance will be less effective than in the case where we use

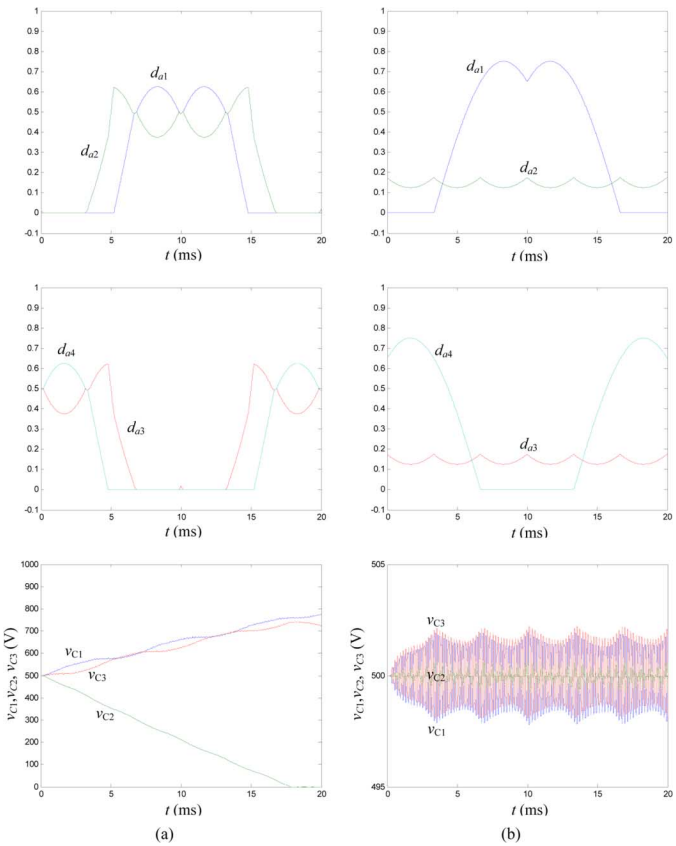

Fig. 6. Simulation results for d_{a1}, d_{a2}, d_{a3}, d_{a4}, v_{C1}, v_{C2} and v_{C3} in the following conditions (scenario 1): $V_{\rm dc} = 1500$ V, $m = 0.75$, $C = 0.5$ mF, $f_s = 5$ kHz, and a linear and balanced load with per-phase impedance $Z_L = 10.5\,\Omega\angle 17.5^\circ$ (series R–L load). (a) Reference NTV PWM. (b) Proposed MTV^2 PWM.

a set of precalculated phase duty-ratios that already guarantee the balance under ideal conditions (this is the case of the proposed MTV^2 PWM). On the other hand, the computation time required by the MTV^2 PWM is significantly lower than the computation time required by the NTV PWM, since no SVD calculations need to be performed (see Appendix). For instance, the computation of 1000 line cycles with $f_s/f_o = 100$ (where f_o is the output fundamental frequency), $m = 0.75$, in a personal computer with an Intel Pentium D processor at 3 GHz, 1 GB of RAM, and using MATLAB 7.2, takes 49.9 s for the NTV PWM and 1.61 s for the MTV^2 PWM. Therefore, the proposed modulation allows a 95% reduction of the computation time, approximately.

In scenario 3, the dc-link capacitors are replaced by regulated dc voltage sources. These sources can be implemented with three ouput-voltage regulated dc power supplies drawing the energy from the dc bus or through the introduction of specific PWM balancing circuits [14], [15]. In this case, the NTV PWM is clearly superior to the MTV^2 PWM from both the point of view of output voltage harmonic distortion and multilevel converter switching losses (see Figs. 7–10). Note, however, that for $m \leq 1/3$, the output voltage distortion and switching losses are the same for both PWMs since they are equivalent for this modulation index range. The only advantage of the MTV^2 PWM is the reduced computation time. Therefore, in this scenario, the use of the proposed MTV^2 PWM may hardly find a practical application.

Finally, in scenario 4, the dc-link capacitors are replaced by unregulated dc voltage sources (e.g., batteries, three separate dc sources obtained from the mains through a bulky low-frequency transformer with multiple secondaries connected to diode rectifiers and filter capacitors, etc.) Again, in this case, the NTV PWM leads to a lower output voltage distortion and lower switching losses. However, if the three dc voltage sources do not have the same voltage value, the use of the proposed MTV^2 PWM prevents from producing low-frequency distortion in the output ac voltages.

In light of the preceding analysis, it is interesting to compare the system in scenario 2 using the MTV^2 PWM (case A), with the system in scenario 3 using the NTV PWM (case B), which a priori seem to be the best candidates when unregulated dc voltage sources are not already available. From Fig. 10 it is clear that case A presents a higher number of switching losses in the multilevel converter than case B, especially for high modulation indexes. Assuming an equal share of conduction and switching losses, this represents a 50% maximum increase in the overall device losses. This increase in switching losses, however, does not occur by increasing the switching frequency of the individual devices, but by extending the portion of the output fundamental cycle where the device is switching, which leads to a better switch utilization and does not typically produce a significant increase in the device junction temperature stress [23]. On the other hand, the extra switching losses in the multilevel converter in case A will typically be lower than the overall losses (conduction, switching, in magnetic and capacitor components) introduced by the additional circuitry in case B, since those additional circuits will have to process a significant portion of the system output energy. From the point of view of output voltage distortion, case A also presents a higher THD than case B. Therefore, in applications requiring a filtering of this distortion the output filter will be bigger and more expensive in case A than in case B. But case A does not require the additional circuitry in case B to generate three regulated dc-link voltage sources. The tradeoff in size and cost will ultimately depend on the modulation index range of operation and filtering requirements. In applications with no stringent filtering requirements such as motor drives, case A is probably the most efficient, compact and less expensive solution.

IV. Experimental Results

Experimental tests have been conducted to verify the performance observed in simulations under scenario 1. A 1-kW prototype has been used for this purpose. The converter is operated in open loop, with a dc power supply connected between dc-link points 1 and 4 and a three-phase series R–L load connected to the ac side. The computation of the nine independent phase duty-ratios is performed by the embedded PowerPC of dSpace DS1103. This information is sent to an Altera EPF10K70 programmable logic device in charge of generating the eighteen switch control signals.

In Fig. 11, it can be observed that the NTV PWM used as a reference for comparison leads to the collapse of the middle capacitor voltage. The same would occur with any other NTV

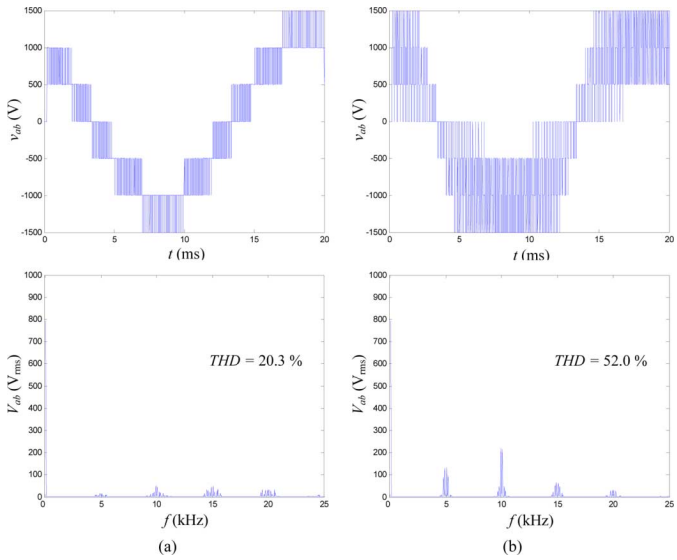

Fig. 7. Simulation results for output voltage v_{ab}, and FFT(v_{ab}) in the following conditions (scenario 3): $V_{\rm dc} = 1500$ V, $m = 0.75$, $C = \infty$, and $f_s = 5$ kHz. (a) Reference NTV PWM. (b) Proposed MTV^2 PWM.

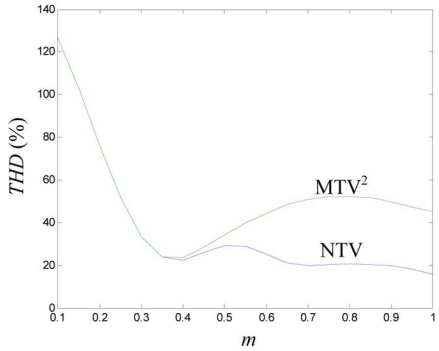

Fig. 8. THD (up to $5 \cdot f_s$) of output line-to-line voltage as a function of m (scenario 3).

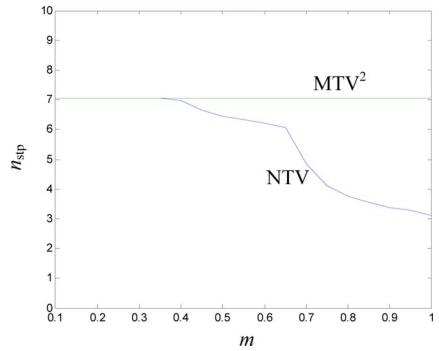

Fig. 9. Fundamental-cycle-averaged number of switching transition pairs per half switching-cycle (n_{stp}) as a function of m.

PWM. On the other hand, in the proposed MTV^2 PWM all three capacitor voltages are fairly balanced in the absence of a closed-loop control. This control, however, is necessary in a real application to guarantee the balance under unequal switching behavior, leakage currents, etc. [22].

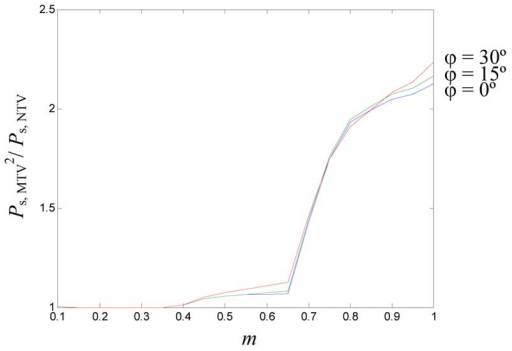

Fig. 10. Ratio of switching losses in MTV^2($P_{s,\rm MTV2}$) and NTV PWM ($P_{s,\rm NTV}$), for different load displacement angles (φ) (scenario 3). The computation of the switching losses has been performed with the same assumptions as in [24], for the same carrier/sampling frequency, and assuming a negligible ac-side current ripple.

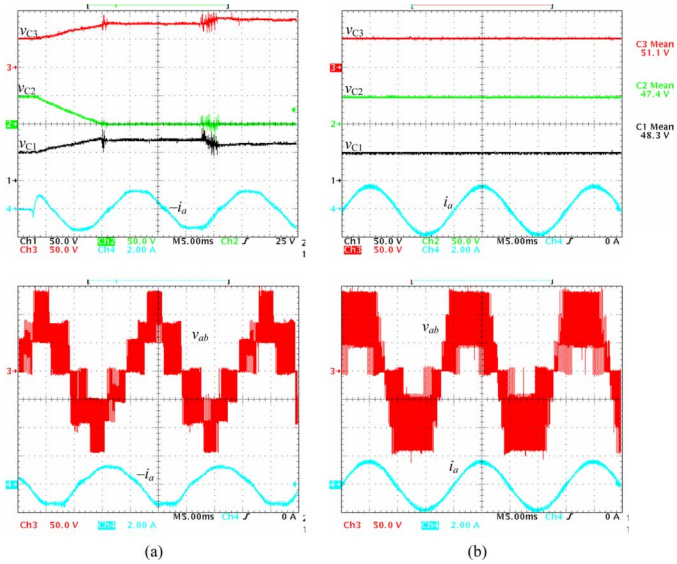

Fig. 11. Experimental results for v_{C1}, v_{C2}, v_{C3}, i_a and v_{ab} in the following conditions (scenario 1): $V_{\rm dc} = 150$ V, $m = 0.75$, $C = 102$ μF, $fs = 5$ kHz, and a linear and balanced load with per-phase impedance $Z_L = 33.5$ $\Omega\angle 8.5°$ (series R–L load). (a) Reference NTV PWM. (b) Proposed MTV^2 PWM.

V. Conclusion

A new modulation approach for the comprehensive control of the dc-link capacitor voltage balance in the four-level three-phase diode-clamped dc–ac converter has been presented (patent pending). The dc-link voltage balancing is achieved for any load (linear or nonlinear, balanced or unbalanced) over the full range of converter output voltage provided that $i_a + i_b + i_c = 0$. Thus, the proposed approach not only enables the use of the four-level diode-clamped converter connected to the output dc bus of a passive front end, but also allows operating with small dc-link capacitors. The dc-link capacitance required to limit the voltage ripple across these capacitors diminishes as the f_s increases.

A practical modulation strategy (MTV^2 PWM) has been defined. The phase duty-ratios of this strategy can be described with simple mathematical expressions, leading to a very compact computation implementation. These expressions are only dependent on the alpha and beta components of the reference

vector. In particular, they do not depend on the load. Therefore, no knowledge of the load is required to implement the proposed modulation.

The proposed MTV^2 PWM has been compared to a conventional NTV PWM under different scenarios.

If the four-level converter is simply connected to a dc bus and operated in open loop, the NTV PWM produces the collapsing of the middle capacitor voltage while the MTV^2 PWM maintains the dc-link capacitor voltage balance under ideal or quasi-ideal operating conditions. In closed-loop, the MTV^2 PWM presents a better dynamical performance and lower computation time, being the converter losses and output voltage THD similar in both cases.

If the dc-link capacitors are replaced by dc voltage sources, the NTV PWM is clearly superior since it presents lower switching losses in the multilevel converter and lower output voltage THD than the MTV^2 PWM.

Finally, in cases where dc voltage sources are not already available, the selection of a system configured by the multilevel converter connected to a single dc bus and operated with the MTV^2 PWM or a system configured by the multilevel converter with dc voltage sources replacing the dc-link capacitors, will depend upon the specific application specifications; in particular, the modulation index range of operation and the filtering requirements.

APPENDIX

ALGORITHM FOR THE COMPUTATION OF THE PROPOSED MTV^2 PWM PHASE DUTY RATIOS*:* In the following, an algorithm to compute the phase duty ratios of the proposed MTV^2 PWM is presented. It is assumed that the inputs of the modulator are the alpha and beta components of the reference vector: $V_{\mathrm{ref}\alpha}$ and $V_{\mathrm{ref}\beta}$.

The first step consists on transforming the reference vector into its first sextant symmetric

$$\begin{aligned}
&\text{sextant} = 1\\
&\mathbf{M}_{-60} = \begin{bmatrix} \frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-\sqrt{3}}{2} & \frac{1}{2} \end{bmatrix}\\
&\quad \text{while } \left((V_{\mathrm{ref}\beta} < 0) \text{ or } \left(V_{\mathrm{ref}\beta} > \sqrt{3} \cdot V_{\mathrm{ref}\alpha} \right) \right) \{\\
&\qquad \text{sextant} = \text{sextant} + 1\\
&\qquad \begin{bmatrix} V_{\mathrm{ref}\alpha} \\ V_{\mathrm{ref}\beta} \end{bmatrix} = \mathbf{M}_{-60} \cdot \begin{bmatrix} V_{\mathrm{ref}\alpha} \\ V_{\mathrm{ref}\beta} \end{bmatrix}\\
&\quad \}.
\end{aligned} \tag{12}$$

Next, the value of parameters d_1, d_2, d_3, and d_4 are computed

$$\begin{aligned}
d_1 &= \left(\frac{\sqrt{3}}{2} \right) \cdot V_{\mathrm{ref}\alpha} - \left(\frac{1}{2} \right) \cdot V_{\mathrm{ref}\beta}\\
d_4 &= \left(\frac{\sqrt{3}}{2} \right) \cdot V_{\mathrm{ref}\alpha} + \left(\frac{1}{2} \right) \cdot V_{\mathrm{ref}\beta}\\
d_2 &= d_3 = \frac{1 - d_4}{2}.
\end{aligned} \tag{13}$$

TABLE III
PHASE DUTY-RATIO COMPUTATION

sextant	Phase duty-ratios		
	Phase *a*	Phase *b*	Phase *c*
1	$d_{a1} = 0$ $d_{a2} = d_2$ $d_{a3} = d_3$ $d_{a4} = d_4$	$d_{b1} = d_1$ $d_{b2} = d_2$ $d_{b3} = d_3$ $d_{b4} = V_{\mathrm{ref}\beta}$	$d_{c1} = d_4$ $d_{c2} = d_2$ $d_{c3} = d_3$ $d_{c4} = 0$
2	$d_{a1} = V_{\mathrm{ref}\beta}$ $d_{a2} = d_3$ $d_{a3} = d_2$ $d_{a4} = d_1$	$d_{b1} = 0$ $d_{b2} = d_3$ $d_{b3} = d_2$ $d_{b4} = d_4$	$d_{c1} = d_4$ $d_{c2} = d_3$ $d_{c3} = d_2$ $d_{c4} = 0$
3	$d_{a1} = d_4$ $d_{a2} = d_2$ $d_{a3} = d_3$ $d_{a4} = 0$	$d_{b1} = 0$ $d_{b2} = d_2$ $d_{b3} = d_3$ $d_{b4} = d_4$	$d_{c1} = d_1$ $d_{c2} = d_2$ $d_{c3} = d_3$ $d_{c4} = V_{\mathrm{ref}}$
4	$d_{a1} = d_4$ $d_{a2} = d_3$ $d_{a3} = d_2$ $d_{a4} = 0$	$d_{b1} = V_{\mathrm{ref}\beta}$ $d_{b2} = d_3$ $d_{b3} = d_2$ $d_{b4} = d_1$	$d_{c1} = 0$ $d_{c2} = d_3$ $d_{c3} = d_2$ $d_{c4} = d_4$
5	$d_{a1} = d_1$ $d_{a2} = d_2$ $d_{a3} = d_3$ $d_{a4} = V_{\mathrm{ref}\beta}$	$d_{b1} = d_4$ $d_{b2} = d_2$ $d_{b3} = d_3$ $d_{b4} = 0$	$d_{c1} = 0$ $d_{c2} = d_2$ $d_{c3} = d_3$ $d_{c4} = d_4$
6	$d_{a1} = 0$ $d_{a2} = d_3$ $d_{a3} = d_2$ $d_{a4} = d_4$	$d_{b1} = d_4$ $d_{b2} = d_3$ $d_{b3} = d_2$ $d_{b4} = 0$	$d_{c1} = V_{\mathrm{ref}}$ $d_{c2} = d_3$ $d_{c3} = d_2$ $d_{c4} = d_1$

Finally, the phase duty ratios are calculated with the simple expressions in Table III.

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Sergio Busquets-Monge (S'99–M'06) was born in Barcelona, Spain. He received the B.S. degree in electrical engineering from the Technical University of Catalonia, Barcelona, Spain, in 1999, the M.S. degree in electrical engineering from the Virginia Polytechnic Institute and State University, Blacksburg, in 2001, and the Ph.D. degree in electrical engineering from the Technical University of Catalonia, in 2006.

From 2001 to 2002, he was with Crown Audio, Inc. He is currently an Associate Professor with the Technical University of Catalonia. His research interests include multilevel conversion, power converter modeling, control and automated design, power factor correction, and EMI suppression techniques.

Josep Bordonau (S'87–M'89) received the M.Sc. and Ph.D. degrees in electrical engineering (with honors) from the Technical University of Catalonia, Barcelona, Spain, in 1984 and 1990, respectively.

He has been Lecturer and Assistant Professor in the Electronics Engineering Department, Technical University of Catalonia, where he has been an Associate Professor since 1991. He has been active in more than 25 research projects with international companies and institutions. He has authored more than 60 journal and conference papers His fields of interest are multilevel conversion and ac power conversion applied to renewable energy systems and energy management systems.

Joan Rocabert was born in Barcelona, Spain. He received the B.S. degree in electrical engineering from the Technical University of Catalonia, Barcelona, Spain, in 2003 where he is currently pursuing the Ph.D. degree in electrical engineering.

Since 2004, he has been a Researcher in the Department of Electronic Engineering, Technical University of Catalonia. His field of interest is power electronics applied to photovoltaic- and wind-energy systems.